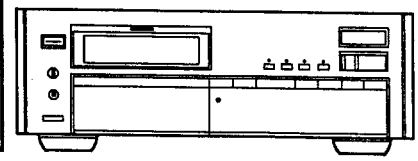
PION-04343

PIONEER
The Art of Entertainment

Service Manual



ORDER NO.
RRV1172

The chapter 1 of this Service Manual will not be reprinted. On your additional orders, we may supply only the chapter 2. For the chapter 1, please make copies and attach to the chapter 2 at your side if necessary.

COMPACT DISC RECORDER

PDR-09

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	Remarks
	PDR-09		
KU	○	AC 120V	

CONTENTS

CHAPTER 1

1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

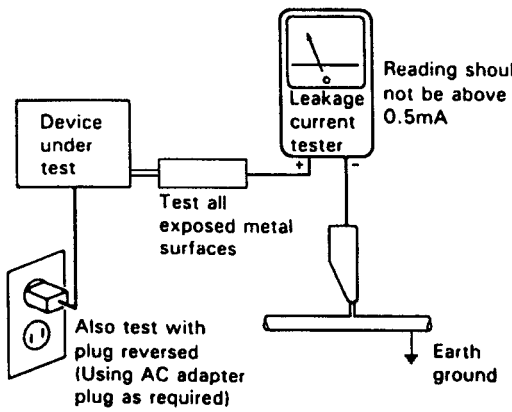
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

1. SPECIFICATIONS

1. GENERAL

Model ..... Compact disc audio system
Applicable discs ..... CDs and CD-Rs
Power supply ..... AC 120 V, 60 Hz
Power consumption ..... 35 W
Operating temperature ..... +5°C to +35°C
Weight (without package) ..... 14.2 kg
Max. dimensions ..... 440 (W) x 445 (D) x 160 (H) mm
17-11/32 x 17-17/32(D) x 6-5/16(H) in

2. AUDIO UNIT

Frequency characteristics ..... 2 Hz to 20 kHz
Playback S/N ..... 112 dB (EIAJ)
Playback dynamic range ..... 97 dB (EIAJ)
Playback total harmonic distortion ..... 0.0026 % (EIAJ)
Playback channel separation ..... 100 dB
Recording S/N ..... 92 dB
Recording dynamic range ..... 92 dB
Recording total harmonic distortion ..... 0.004 %
Output voltage ..... 2 V
Wow-flutter ..... Less than measurement limit
(±0.001% W.PEAK) (EIAJ)
Number of channels ..... 2 channels (stereo)
Digital output ..... Coaxial output: 0.5 Vp-p ±20% (75 Ω)
Optical output: -15 to -20 dBm (wavelength: 660 nm)
Frequency deflection: Level 2 (standard mode)

3. INPUT JACKS

Optical Input jacks (3 system)
Coaxial digital input jack
Audio LINE input jack

4. OUTPUT JACKS

Optical digital output jack (2 system)
Coaxial digital output jack
Audio LINE output jack

5. RECORDING FUNCTIONS

- Recording
- REC MUTE
- AUTO SPACE MUTE:
- AUTO TRACK INCREMENT
- AUTO REC/PAUSE
- Remaining recording time display
- Peak Margin display
- PREVIOUS
- MANUAL TRACK INCREMENT
- MANUAL INDEX INCREMENT:
- INPUT SELECTOR
- TOC Write
- Recording cancellation

6. PLAYBACK FUNCTIONS

- PLAY
- PAUSE
- STOP
- MANUAL search
- TRACK search
- INDEX search
- Direct song selection
- 1 Track repeat
- All track repeat
- Programmed repeat
- Programmed playback (max. 24 tracks)
- Program check
- Program correction
- Program clear
- Pause programming
- Reserved program
- SKIP playback
- DISPLAY OFF
- TIME display switching

7. ACCESSORIES

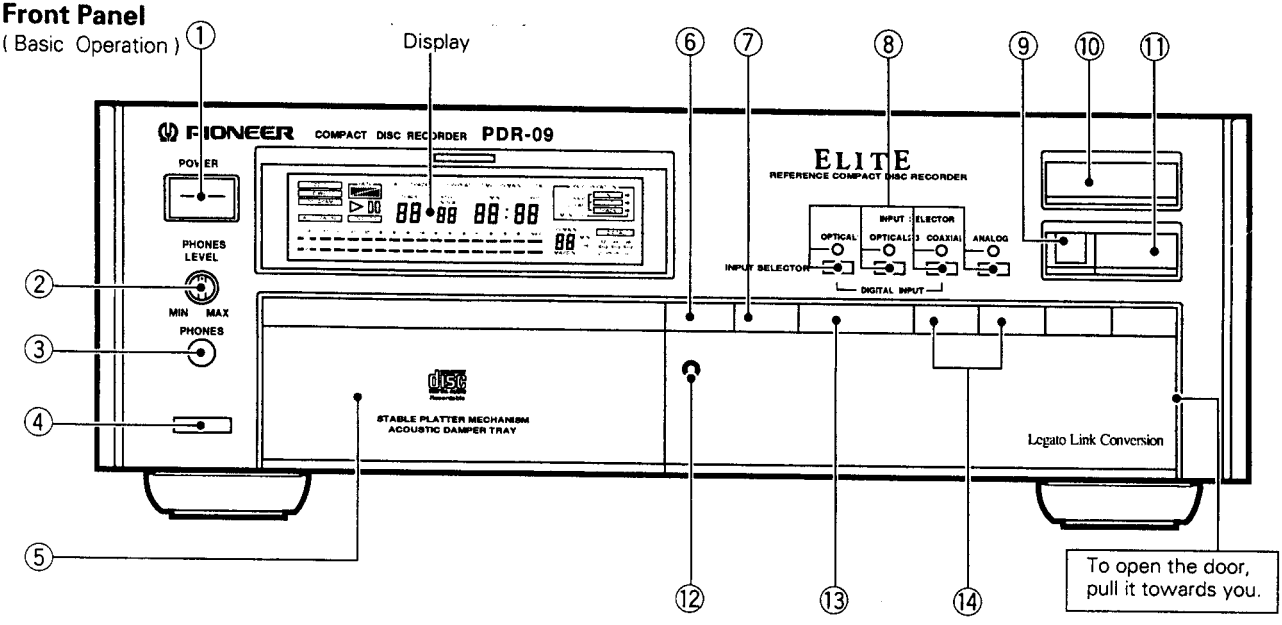
- Remote control unit (CU-PDO57) 1
- Size AAA/R03 dry cell batteries 2
- Audio cable 2
- Control cable 1
- Turntable sheet 1
- Operating Instructions 1

NOTE:

The specifications and design of this product are subject to change without notice, due to improvements.

2. PANEL FACILITIES

Front Panel
(Basic Operation)



Buttons for basic operation

① POWER switch

Pressing this button switches the power ON. Pressing it again switches the power OFF.

NOTE:

Be sure to remove the CD - R disc before switching the power OFF. Otherwise important data such as TOC and SKIP information may be deleted.

② PHONES LEVEL adjustment knob

③ PHONES jack

④ Remote control receiver

⑤ Disc tray

To load a CD or CD - R.

⑥ OPEN/CLOSE (▲) button

To insert/remove a CD or CD-R. The disc tray ejects/retracts each time this button is pressed.

⑦ STOP (■) button

Press to stop recording or playback. Pressing this button terminates all operations of the system (Stop). If this button is pressed while the system is stopped and when a program has been input, the program will be cleared (Clear).

⑧ INPUT SELECTOR button and indicator

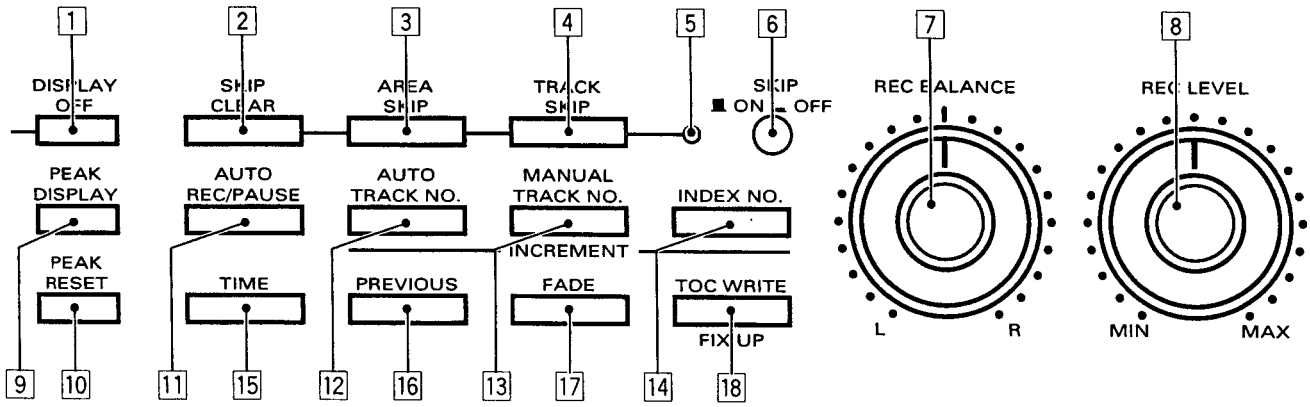
To select an input source to be recorded. The input source must be selected for both digital and analog inputs. The indicator lights up when the button is pressed.

OPTICAL 1: To record from an equipment connected to the digital OPTICAL 1 input jack.

OPTICAL 2/3: To record from an equipment connected to the digital OPTICAL 2 or 3 input jack. (Changeover between OPTICAL 2 and 3 is performed by means of the switch on the rear panel. Refer to Page 12.)

COAXIAL: To record from an equipment connected to the digital COAXIAL input jack.

ANALOG: To record from an equipment connected to the (analog) LINE IN jack.



⑨ REC (●) button
Press to switch the system to REC/PAUSE mode. The REC and PAUSE indicators light up. To start recording, press the PLAY (►) or PAUSE(II) button.

⑩ PAUSE (II) button
Press to pause the system during recording or playback. To resume operation, press the button again.

⑪ REC MUTE (O) button
Press during recording to create a 4 - second blank and pause the system.
Holding down this button creates a break as long as it is pressed. Releasing the button pauses the system.

⑫ DISPLAY OFF indicator
Lights up when all indicators are off.

⑬ PLAY (►) button
Press to play back a disc or start recording.

⑭ TRACK search button
Press to search a desired title during playback (or programmed playback) or pause. Pressing this button forwards to the next song or reverses to the previous song.

⑮ MANUAL search button
Press to fast forward or reverse during playback or pause. The system continues fast forward/reverse as long as the button is held down.

[1] DISPLAY OFF button
Press to turn the display off (see "To turn the display off" on page 30). To prevent influence on the sound quality, the system deactivates all circuits not in use while the display is turned off.

[2] SKIP CLEAR button
Press to delete SKIP information.

[3] AREA SKIP button
Press to specify areas to be skipped during playback.

[4] TRACK SKIP button
Press to specify tracks to be skipped during playback.

[5] SKIP ON/OFF indicator
Light up to indicate that SKIP information can be input/cleared (SKIP OFF).

[6] SKIP button
ON :Press out to enable SKIP playback.
OFF :Press in to disable SKIP playback so that SKIP information can be input.

[7] REC BALANCE adjustment knob
Turn to adjust the balance (L and R) of the input level when recording analog signals.

[8] REC LEVEL adjustment knob
Turn to adjust the recording level in accordance with the input source when recording analog signals.

[9] PEAK DISPLAY button
Press to switch between Peak Margin display and Remaining Recording Time display.
- The Peak Margin display shows the margin of the input level to the maximum allowable input in "dB".
- The Remaining Recording Time display shows the time recordable for the CD-R.
  During TOC recording, the display shows the time required for completion of TOC recording in minutes.

[10] PEAK RESET button
Press to reset the Peak Margin. When the button is held down, the system shows the margin in real time.

[11] AUTO REC/PAUSE button
Press to automatically start/stop recording when copying a CD, CD - R or MD to a CD - R disc by using digital signals. During digital recording from other sources, the system automatically stops recording 30 seconds after a blank (no signal) is detected.
When recording analog signals, the system automatically stops recording 60 seconds after the source equipment stops playback.

[12] AUTO TRACK NO. INCREMENT button
Press to automatically update recording track numbers in sequence when recording to CD - R discs.

CAUTION:
This function differs during digital and analog recordings. It also differs, depending on the source equipment.

[13] MANUAL TRACK NO. INCREMENT button
Press to manually update recording track numbers when recording to CD - R discs.

[14] INDEX NO. INCREMENT button
Press to manually update recording index numbers when recording to CD - R discs.

[15] TIME button
The time display changes in the sequence of TIME, REMAIN and TOTAL each time the button is pressed.

[16] PREVIOUS button
Press to confirm the final recording condition and the recording end point (for example, when additional recording is required).

[17] FADE button
Press to fade in or fade out during recording or playback. Also, use this button to set the fade time.

[18] TOC WRITE button
Press to write TOC information to CD - R discs. Once TOC information is written, the CD - R discs can be played back with normal CD players.

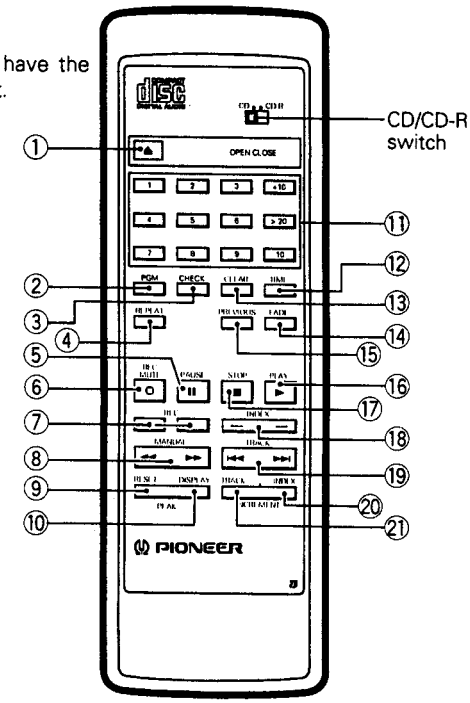
IMPORTANT !

After TOC information is written to CD - R discs, they cannot be used for further recording.

• REMOTE CONTROL UNIT

Remote control unit

* The button of the remote control unit have the same functions as those on the main unit.



① OPEN/CLOSE button (▲)

② PGM (program) button
For programmed song selection.

③ Check button
To check a program.

④ REPEAT button
For repeated playback.

⑤ PAUSE (II) button

⑥ REC MUTE (O) button

⑦ REC (●) buttons
Pressing the two buttons simultaneously switches the system to REC/PAUSE mode.

⑧ MANUAL search button

⑨ PEAK RESET button

⑩ PEAK DISPLAY button

⑪ Digit buttons (1 to 10, + 10 and > 20)
To specify title numbers for direct or programmed song selection.

⑫ TIME button

⑬ CLEAR button
To delete a program.

⑭ FADE button
To fade in or fade out during recording or playback.

⑮ PREVIOUS button

⑯ PLAY (►) button

⑰ STOP (■) button

⑱ INDEX search button
To search a break between musical portions or between songs (index) during playback or pause.

⑲ TRACK search button

⑳ INDEX NO. INCREMENT button

㉑ MANUAL TRACK NO. INCREMENT button

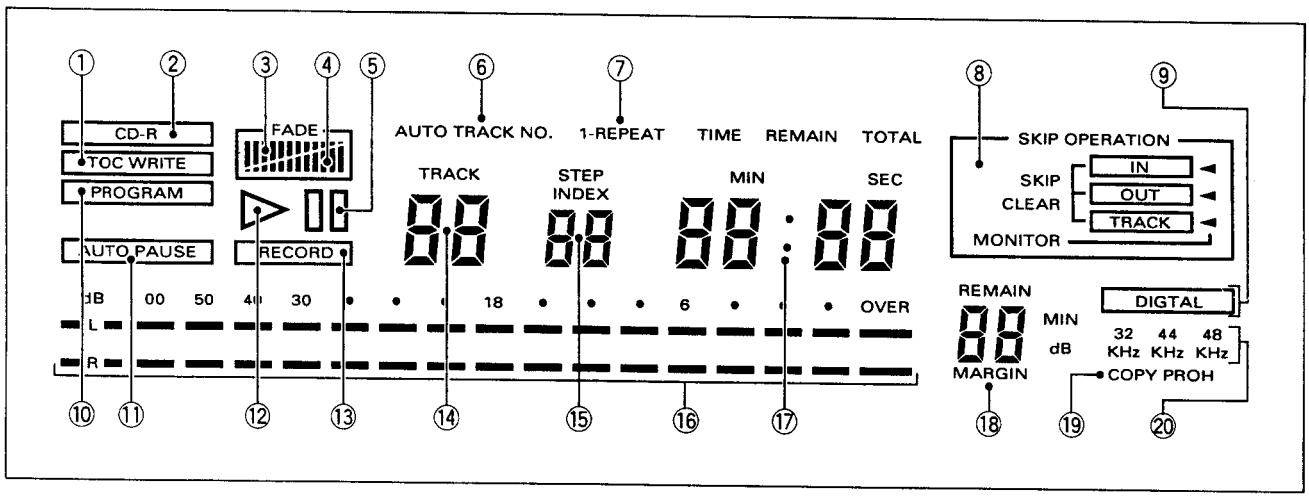
CD/CD-R switch

CD : The remote control unit can be operated with other Pioneer CD players having the SR symbol.

CD-R : Select this setting for using the remote control unit only for this unit.

• Be sure to set the CD/CD-R switch on the rear panel of this unit (see page 9) to the same setting as with CD/CD-R switch of the remote control unit.

• DISPLAY



①Lights up when writing TOC information to CD - R discs. Blinks when TOC information is required to be written.
②Blinks while the system identifies the disc. Lights up when CD - R discs are used.
③Blinks during fade - out and during input of the fade - out time.
④Blinks during fade - in and during input of the fade - in time.
⑤Lights up during pause.
⑥Lights up when the system enters Auto Track Number mode.
⑦Lights up when the system enters repeat playback mode.
⑧Lights up, turns off and blinks when SKIP information is input/cleared.
⑨Lights up if digital input is locked during recording mode.
⑩Lights up when the system enters program mode.
⑪Lights up when the system enters AUTO REC/PAUSE mode.
⑫Lights up during playback.
⑬Lights up during recording. Blinks when the system enters Recording Mute or Recording Monitor mode.
⑭Displays the track number.
⑮Displays the index or program steps.
⑯Displays the peak value of the input level during recording. Displays the peak value of the playback level during playback. (See page 21.)
⑰Displays the elapsed playback time, remaining playback time, total playback time, elapsed recording time, remaining recording time, total recording time, relationship between the start and end points for area SKIP input, points for area SKIP input, and remaining time until end of TOC data recording.
⑱Displays the remaining recording time and the peak margin during recording. Displays the total remaining playback time during playback, and the total programmed playback time during programmed playback. Displays the remaining time for completing TOC writing.
⑲Lights up or blinks when the system detects the digital signal to disable recording, as specified by SCMS.
⑳Displays the current sampling frequency (Fs) of the digital input. All three indicators turn off if the input signal is interrupted during digital recording.

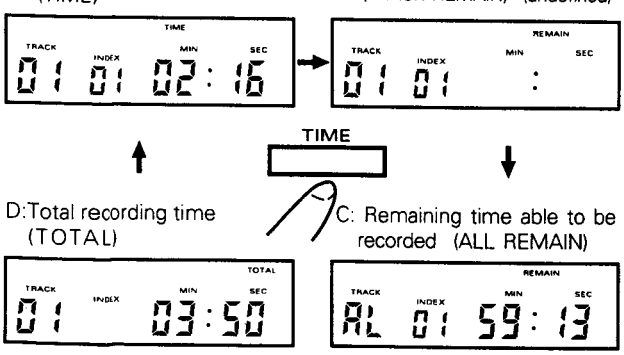
Switching the time display

The time display can be switched to check the recording time during recording, and the playback time during playback.
The display changes in the sequence of A, B, C and D each time the TIME button is pressed.
Note that the time during recording is displayed in a different way from the time during playback

Recording

A: Elapsed recording time (TIME)

B: Remaining time of the song being recorded (TRACK REMAIN) (undefined)



TIME

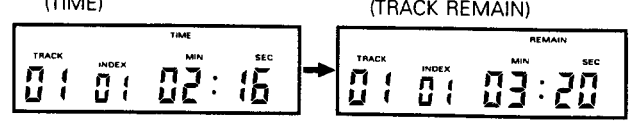
D:Total recording time (TOTAL)

C: Remaining time able to be recorded (ALL REMAIN)

Playback

A: Elapsed playback time (TIME)

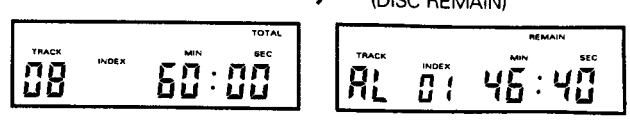
B: Remaining time of the song being played back (TRACK REMAIN)



TIME

D: Total playback time (TOTAL)

C: Remaining time of the disc being played back (DISC REMAIN)



4. DISASSEMBLY

• Use of 13P F.F.C. for Service

When servicing the unit (adjusting the pickup assy or repairing the head board assy) after setting the head board assy in a standing position (Fig. 1) by inserting it into the P board holder (PNY - 405), use 13P F.F.C. to connect the head board assy and the spindle motor.

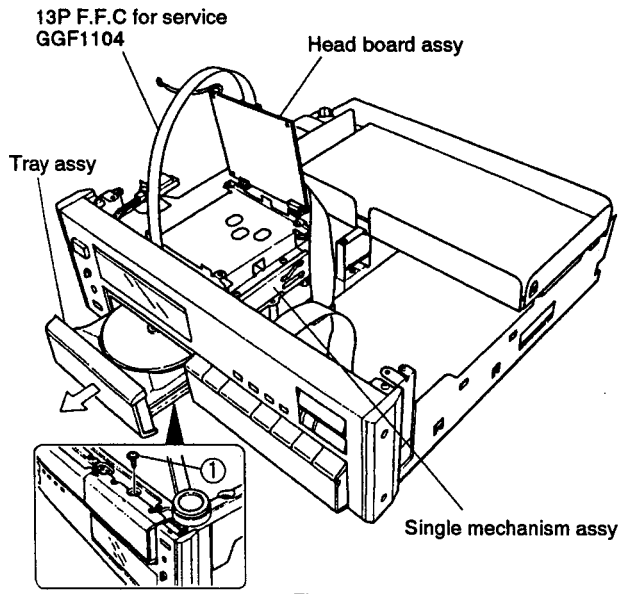


Fig. 1

• Removing the Tray Assy

1. Turn on the power and press the OPEN/CLOSE button to open the tray assy.
2. Remove the fixing screw ① of the tray assy (Fig.1).
3. Grip the tray by hand and slowly pull it out from the unit.

Notes 1 To open the tray manually

- You can slowly pull out the tray assy as long as the servo mechanism assy is not in its lower disc-clamp position. Be sure to turn off the power before pulling on the tray.
- If the tray does not move or stops part way when you try to pull it out, follow the procedure below to set the servo mechanism assy to its upper position where the disc is not clamped.

1. Remove top plate R (fixed by a screw ②), then top plate F (fixed by a screw ③). (Fig. 2)
2. With both hands, push on the cams ④ (one each on the right and left) of the single mechanism assy, at the position indicated by arrow Ⓐ in Fig. 3 (the position is the same with the other cam), fully towards the front panel.

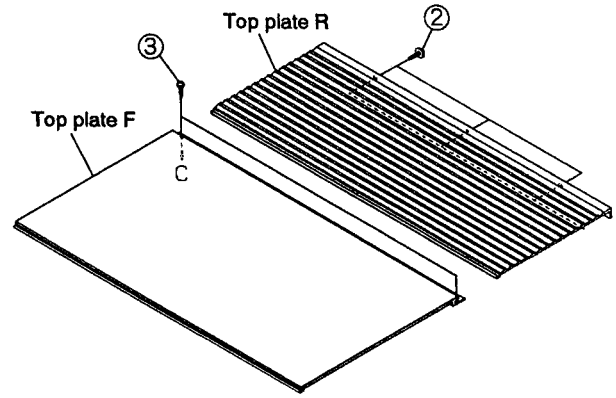


Fig. 2

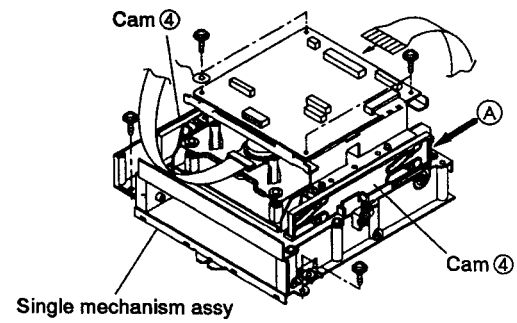


Fig. 3

3. Slowly pull out the tray assy to open.

• Removing the Servo Mechanism Assy

1. Solder and short - circuit between the patterns in block Ⓑ of the PU flexible board of the pickup assy.
2. Disconnect connectors Ⓒ to Ⓖ of the head board assy.
3. Disconnect earth lead Ⓗ (fixed by a screw).
4. Remove the mechanism cover ⑦ (fixed by two screws each on the left and right) while leaving the head board assy in place.

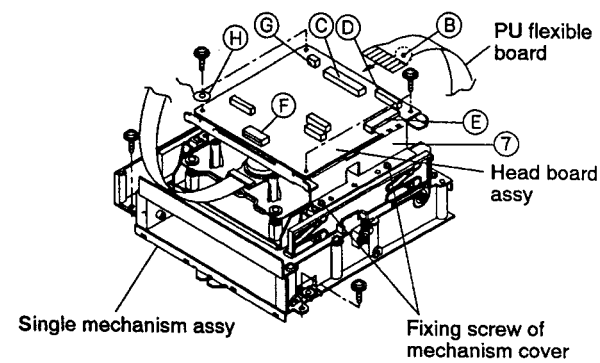


Fig. 4

5. Remove the four fixing screws ⑧ of the servo mechanism assy (Fig. 5).
6. Pull up and remove the servo mechanism assy, taking care not to lose its float springs.

Note: The four float springs are of different colors for their respective mounting positions. When reassembling, note the correspondence between the colors and the positions. Be careful not to damage the PU flexible board, as it is not secured in place.

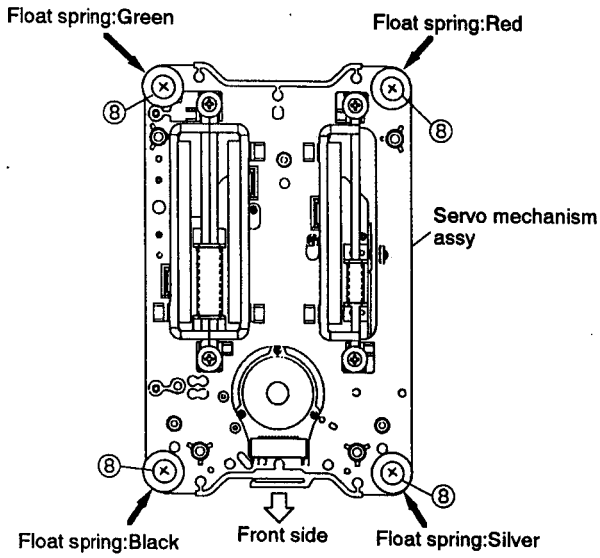


Fig. 5

• Removing the Pickup Assy

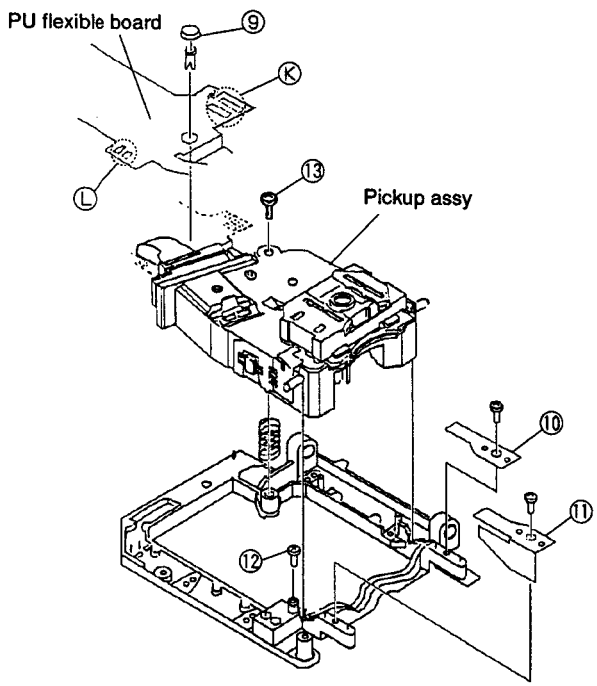


Fig. 6

1. Disconnect the lead wires of the drive coil and speed-detection coil, which are soldered to blocks Ⓚ and Ⓛ of the PU flexible board.
2. Remove the rivet ⑨ which holds the PU flexible board.
3. Remove plate springs S ⑩ and L ⑪ (each fixed by a screw and screw ⑫).
4. Remove the adjustment screw ⑬.

• Removing the Audio Board Assy

1. Remove top plate R, top plate F, the right and left side boards and the rear panel to obtain the condition shown in Fig. 7. (A 2-mm diagonal hexagonal wrench is required to remove the side boards).
2. Disconnect the all connectors connected to the audio board assy and connector Ⓡ of the power supply board assy.
   (Remove connector Ⓡ by pinching it with the fingers.)
   Loosen cord holder and remove wire.
3. Remove the seven fixing screws of the shield case and slowly pull up and remove the shield case (audio board assy).

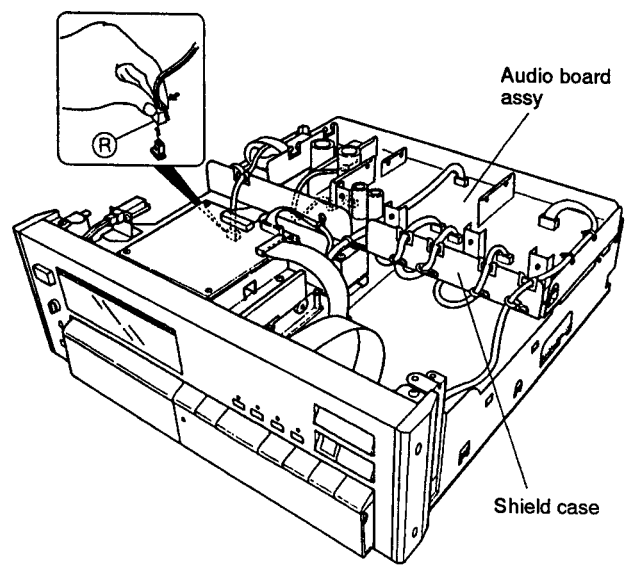


Fig. 7

5. CIRCUIT DESCRIPTION

5.1 CD-R DISC

As shown in Fig. 5 - 1, the disc for CD-R (compact disc recorder) is constructed from a resin board as base, with a recording layer, reflection layer, and protection film made from pigment film respectively layered on top. Guidance slots called "grooves" are cut into the top of the disc. When a strong laser beam is applied to these grooves during recording, the pigment quality changes and generates a recording pit. These grooves also have "wobble" or surges in the constant frequency which serves as the base for control of the number of disc revolutions. This wobble undergoes FM modulation to allow you to obtain information such as the absolute time of the disc.

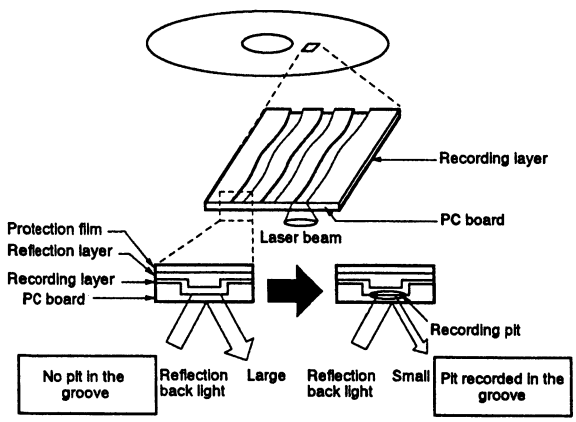


Fig. 5-1

objective lens where it is again converted into parallel light. The light then passes through the reflection and quadrangular prisms to the convex lens. It then continues on to the multi lens where astigmatism occurs after which it enters the 8 divided photodiode. The center section of the photodiode sectioned into 4 divisions creates the information and focus signals, and all three sections combine to create the tracking signal as is shown below.

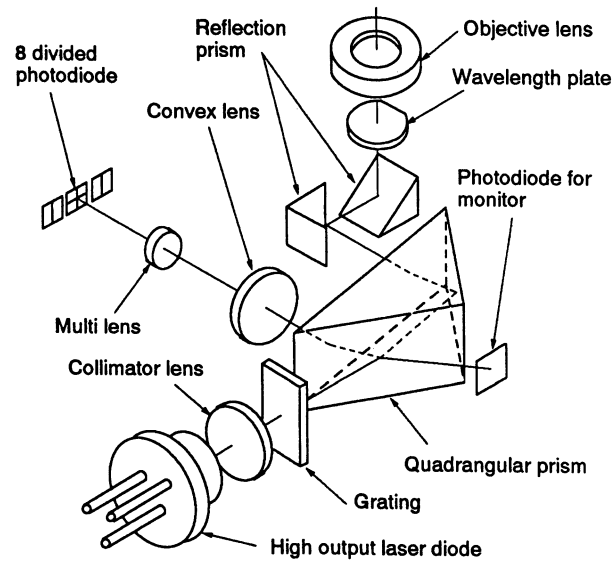


Fig. 5-2

5.2 PICKUP

5.2.1 Optical Path in the Pickup

The interior of the pickup is configured as shown in Fig. 5 - 2. The difference between a normal CD pickup and pickup for recording is that the recording pickup has an optical system that has an infinite amount of lines in order to increase the emission power of the objective lens, and that a high-output type laser diode is used.

The following is an explanation of the flow of light using the optical path diagram as a guide. First, the light emitted from the laser diode is converted into parallel light by a collimator lens. It then passes through a grating and is divided into three beams which proceed toward the quadrangular prism. A portion of the beams enter the quadrangular prism and spread into an ellipse after refracting from the plane of incidence of the prism. The remainder of the beams is reflected to the photodiode for monitor and used to control the laser diode power.

The light that passes through the quadrangular prism proceeds through the two reflection prisms and wavelength plate to the objective lens where it is converged on three spots on the disc.

The light is then reflected from the disc and back to the

5.2.2 Servo System

The law of astigmatism is used by a focus servo in the same manner as with a normal CD, however this unit cannot use the 3-beam method used in a CD in relation to the tracking servo. The reason being that the 3-beam method requires the servo to read the bright light on a disc, and the servo cannot read a disc that is completely light before recording. As a result, the push-pull configuration shown in Fig. 5 - 3 is used in the pickup of existing compact disc recorders. A push-pull configuration uses the light diffracted from the grooves back to photodiode to acquire tracking signals by taking the difference of the left and right of the returned light. However, offset occurs in one of the push-pull signals through the curve of the disc or fluctuations that follow the objective lens. To eliminate the offset, this unit uses the tracking system shown in Fig. 5 - 4. This system eliminates offset using the "differential push-pull method" which mixes the push-pull signals from the three light beams.

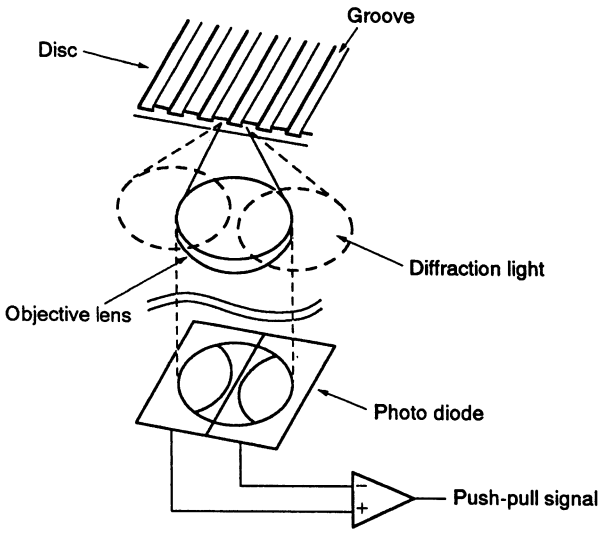
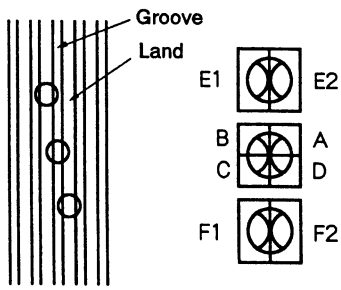


Fig. 5-3



Beam position on the disc PD shape

$$TE = [(A + D) - (B + C)] - \frac{K}{2}[(E2 - E1) + (F2 - F1)]$$

(K=0 – primary light ratio)

Fig. 5-4

5.3 SERVO SECTION

5.3.1 APC

Control of the laser power varies according to the operation mode (playback or record). In playback mode, this unit basically uses the same APC (Automatic Power Control) as a CD player, but in recording mode, a different APC is used.

In playback mode, the signal that detected the output power of the pickup's laser diode is input from MD (pin 23) in the RF amp IC (IC101: PA4020A), converted from current to voltage (I/V), and amplified. Next, this signal is compared with the VR103 voltage determining the playback power and the resulting signal is input to the voltage-current (V/I) conversion circuit configured with the operation amp and Q102 and Q110 and added to the laser diode. The laser power is normally constant in regard to temperature fluctuations because the circuit works so that the detection current of the monitor diode is constant, the laser power is always constant in regard to temperature fluctuations.

In recording mode, the laser power necessary for recording is generated only when creating a pit with the APC during playback working. However, so that level fluctuations in the servo signals do not occur during recording, this unit is constructed to operate the playback APC on a laser power signal when the sample hold circuit of the RF amp IC has not created a pit.

It is necessary that the recording power be separately maintained at the most suitable value due to fluctuations caused by dispersion on the disc (OPC adjustment). This value is converted into voltage by the D/A converter

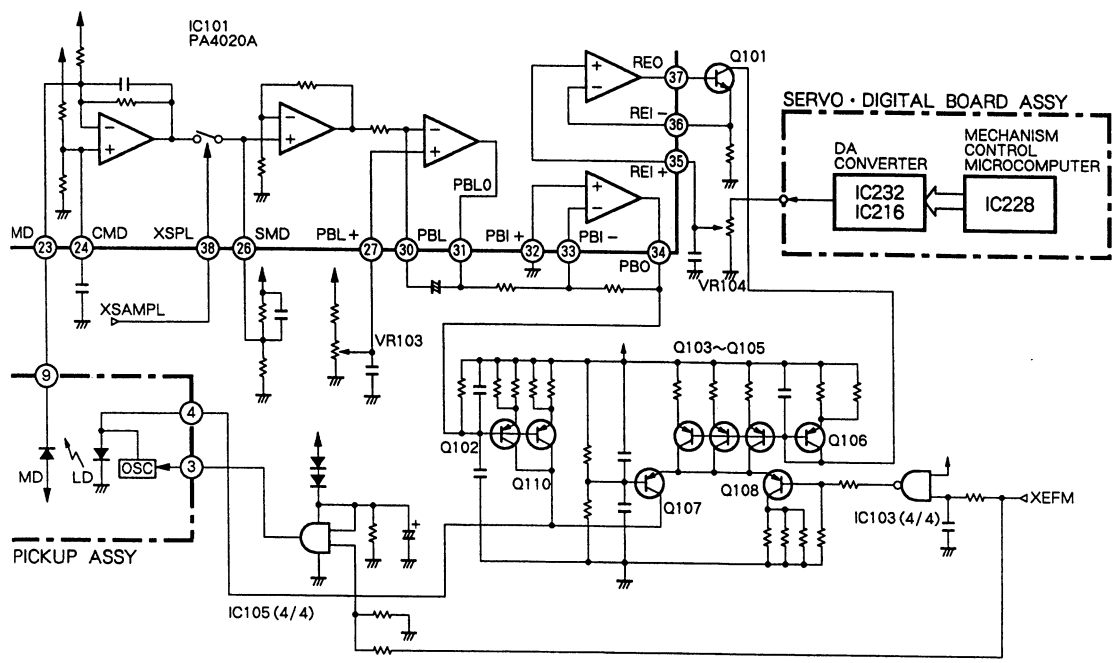


Fig. 5-5 Periphery APC circuit

configured from IC232 and IC216, and input from the mechanism-control microcomputer (IC228: UPD78323GJ - 5BJ) in the Servo•digital board assy to the operation amp in the RF amp IC and the Q101 V/I conversion circuit. The current is then amplified by the mirror circuit configured from Q103 through Q106 and added to the laser diode from the collector in Q107. This current is controlled (ON/OFF) from IC103 and Q108 with the recording signal from the EFM encoder IC (IC311: LC89583) and creates a pit string on the disc.

High frequencies are normally applied to the laser diode in an ordinary CD player, however to protect the laser diode in this unit, a high frequency is not applied when recording power outputs timing via IC105.

5.3.2 Error Signal Generation Circuit

The pickup has one main beam 4-division detector and two sub-beam 2-division detectors that use the 3-beam differential push-pull method. The output current is converted into voltage (I/V conversion) every output as shown in Fig. 5 - 6 in order to generate HF, RF, wobble, focus error, and tracking error.

The signals output from detectors A, B, C, D, E1, E2, F1 and F2 are input to pin 14, pin 22, pin 19, pin 17, pin 20, pin 21, pin 16, and pin 15 of RF amp IC respectively, converted from current into voltage (I - V), and directed to the sample hold circuit. The sample hold circuit is designed to stabilize and create each error signal during recording. When a pit has not been created, the sample hold circuit performs sampling, and when a pit has been created (when the laser emits recording power), it holds sampling.

After sampling hold circuit output has been amplified, the HF, RF, and focus error signals are generated by computing the main beam output in the same manner as a CD player. These signals are then output to pin 66, pin 68, and pin 55 respectively.

As shown in Figu. 5 - 7, the offset of a focus error signal is adjusted by VR105 connected to pin 56, and the offset fluctuations caused by temperature are cancelled by the R148 temperature compensation resistor.

As shown in Fig. 5 - 8, a tracking error generates main and sub beam push-pull signals by adding and subtracting these signals. The light balance of the main and sub beams is adjusted by VR110 connected to pin 48 and output to pin 49. After the gain and offset of this output have been adjusted by VR111 and VR112 respectively, the output is re-input to the RF amp IC from pin 50, and amplified. Finally, the signals are output to pin 51 in the following form.

$$[(A+D) - (B+C)] - K[(E2 - E1) + (F2 - F1)] / 2$$

(K=0 - primary light ratio)

The wobble generation circuit is shown in Fig. 5 - 9. Wobble signals are computed from a main beam as [(A+D) - (B+C)] and output from pin 61. Also, the auto balance circuit works to acquire quality wobble signals in order to prevent against an inferior C/N because the left and right balance is broken due to disc eccentricity or optical axis aberration and the RF must be cancelled.

This circuit passes the previously-stated computed output through the inversion amp whose band is limited to the maximum frequency of the eccentricity. The circuit is configured to feed back this output to the voltage control resistor (IC102: CXD7500M) which is connected to the computation circuit on the first stage.

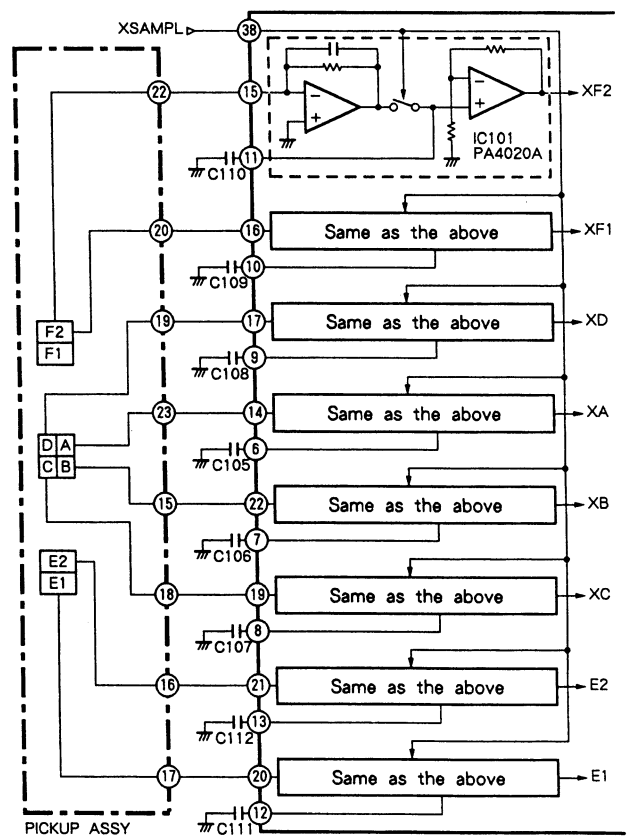


Fig. 5-6 I/V Conversion circuit

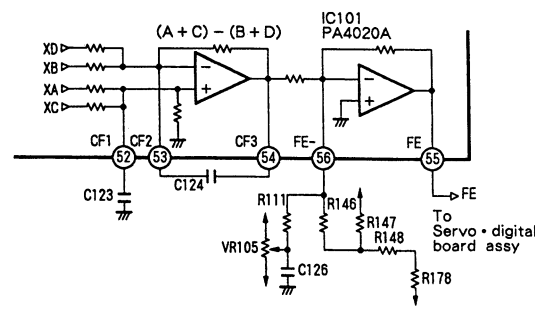


Fig. 5-7 Focus error generation circuit

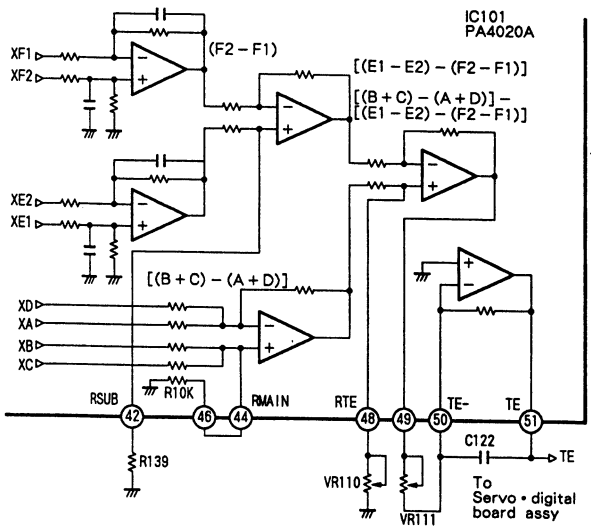


Fig. 5-8 Tracking error generation circuit

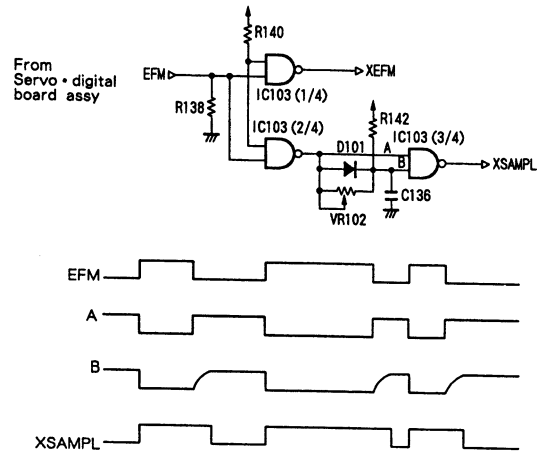


Fig. 5-10 Sample hold pulse generation circuit

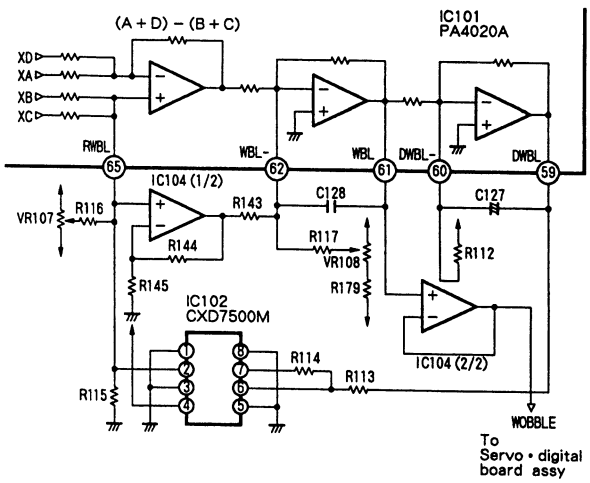


Fig. 5-9 Wobble generation circuit

5.3.3 Sample Hold Pulse Generation Circuit

In recording mode, the laser power is at a recordable level only when pits have been created. This helps to avoid a normal servo when the light reflected from the disc changes in pit creation and playback level modes. A sample hold method, which uses a signal in playback level mode only, is used to counter the problem of different levels of reflected light.

The sampling pulses are L level signals that span from 500 nsec after the falling edge to the rising edge of the recording EFM signal. The waveform of the recording EFM signals made in the Servo • digital board assy are shaped by IC103 (1/4). Some of the signals are directly input to the NAND gate [IC103 (3/4)] through the CR circuit, but the remainder are delayed in regard to the EFM signal and then input. This output is input to pin 38 of the RF amp IC as XSAMPL of the sample hold pulse.

5.3.4 Focus Servo

As shown in Fig. 5-11, the focus servo system of this unit is identical to that of a CD player. The error signals created by the RF amp IC are directed to the Servo•digital board assy through CN106. The loop gain of these signals is adjusted by VR201 and they are input to FXC (pin 46) and FE (pin 47) in the CD servo control IC (IC201: CXA1372Q). These signals are then output from FEO (pin 5) through the defect countermeasure and phase compensation circuits in the IC. Next, this output is directed to the Head board assy and added to the focus actuator drive coil by the power operation amp (IC106: LA6517).

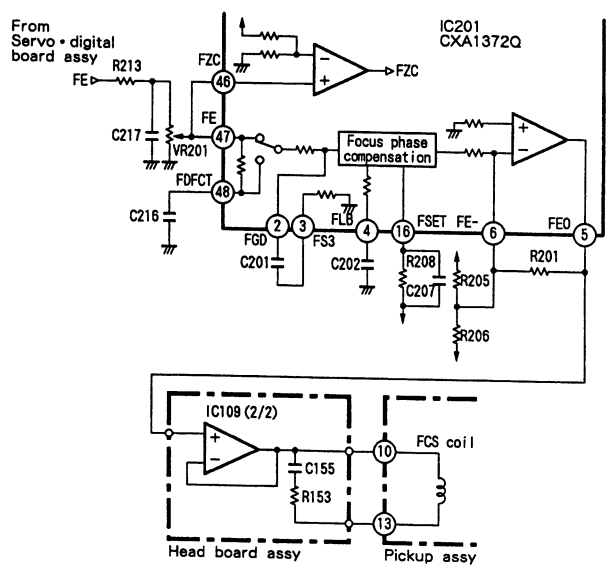


Fig. 5-11 Focus servo circuit

5.3.5 Tracking and Sled Servo

As shown in Fig. 5 - 12, the tracking servo system of this unit is identical to that of a CD player except that gain adjustments are controlled from the mechanism - control microcomputer. Error signals generated by the RF amp IC are directed to the Servo • digital board assy through CN106 and input to the variable gain amp configured from IC202 and IC203 (1/2). This supports TRK error gain dispersion on each disc and provides the best loop possible. For the gain settings, the tracking servo should be open and the control signals input to pin 9, 10, and 11 of IC202 is sequentially changed by the mechanism-control microcomputer. As a result, amplification of the tracking error output of IC203 (1/2) is also sequentially changed. The output is then clamped to a constant direct current level by the circuit consisting of IC211(1/2), C272, and D203, converted into direct current voltage by IC221 (2/2) half wave rectifier, and input to the mechanism-control microcomputer. The criterion level varies according to the disc type used, however the IC202 control signal is set so that the gain is determined by the microcomputer at the optimum level in relation to the voltage.

The output from the variable gain amp adjusts the loop gain via VR202 and is input to TE (pin 43) of the CD servo control. This output is then passed through the defect and phase compensation circuits in the IC and output from TAO (pin 11). Next, the output is directed to the Head board assy and added to the tracking actuator drive coil from the power operation amp (IC106 : LA6517).

TAO output passes through the low-pass filter (LPF) and into SL + (pin 13) of the CD servo control IC. A linear motor allows for this output to also be used as input for the sled servo system, just as in the setup of a normal CD player. The slider control signals output from SLO (pin 14) are directed to the Head board assy via CN201, and input to IC107 (1/2) in the speed control loop. In IC107 (1/2), the gain and phase compensation for the speed control loop is performed, the circuit offset is cancelled by VR101, and this output is added from the driver IC [IC109 (1/2)] to the linear motor coil in the slider.

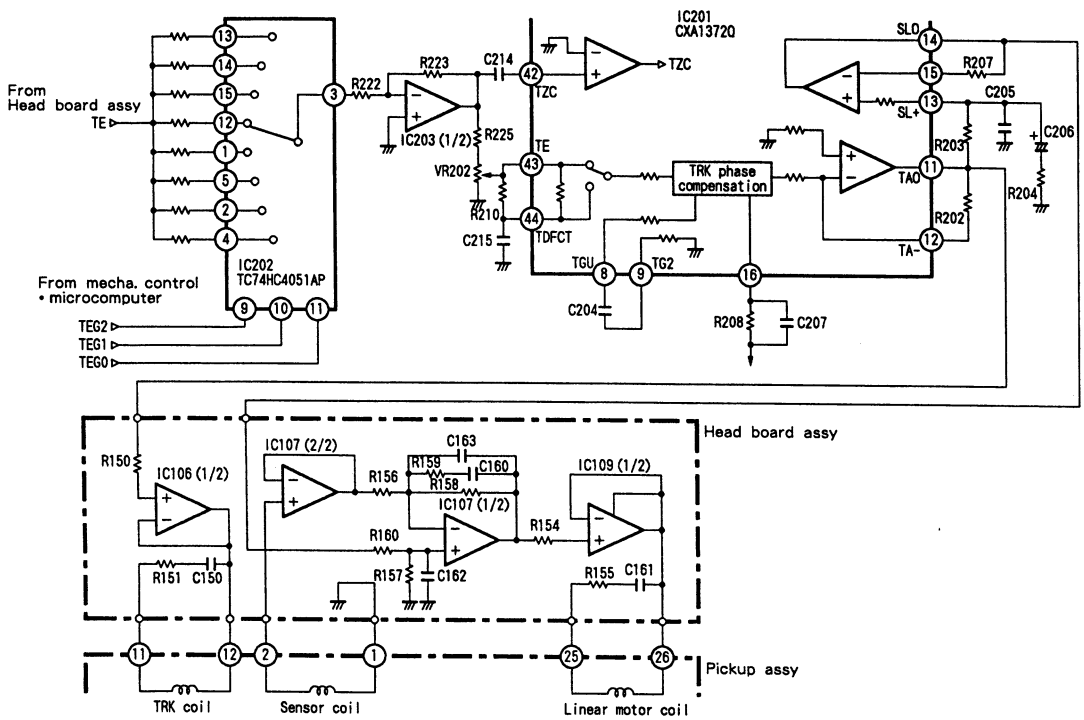


Fig. 5-12 Tracking servo circuit

5.3.6 Spindle Servo

A block diagram of the spindle servo is shown in Fig. 5-13. The spindle motor controls are individually controlled during recorded section only playback mode, blank (unrecorded) section playback mode, recording mode and disc revolution change mode as described below.

First, control in recorded-section-only playback mode is identical to that of a CD player. RF signal generated by the RF amp IC are directed to the Servo•digital board assy through CN106 and input to RFI (pin 39) of the CD servo control IC. The input RF signal is converted into binary signals by a comparator and output to EFM (pin 32), after which they are input to RF (pin 24) of the CD decoder IC (IC225: CXD2500BQ) where MDS and MDP error signals are generated from sync and internal reference signals (including EFM signals). Processing by this IC is completely digital. The final step in creating a spindle control signals is when a ternary PWM signal is output to MDP (pin 4) and the carrier portion is removed by the IC203 (2/2) filter.

Next, blank section playback and recording modes do not have the sync signal mentioned above, instead the disc revolution control signal known as "wobble" is read from the grooves cut into the disc. Also, ATIP (absolute time information processing) can be acquired from these signals as described below.

After setting the number of spindle motor revolutions to the desired speed using CAV (Constant Angular Velocity) speed which uses PWM output from the mechanism - control microcomputer, the servo is changed to the spindle servo using the wobble. The wobble servo directs the wobble signals generated by the RF amp IC to the Servo • digital board assy via CN106, and the unnecessary portions of the signal are removed by the 22.05 kHz band-pass filter (BPF) configured from IC219 and IC220 (1/2).

Next, the signals are converted to binary by a comparator [IC207 (2/2)] and input to WOBBLE (pin 21) of the ATIP decoder IC (IC222: G307PA23).

The 4.3218 MHz supplied from the EFM encoder IC serves as the master clock signal. This IC compares the phases of the master clock signal divided into 22.05 kHz and the wobble signals above, and then outputs binary PWM signals. The final step in creating a spindle control signal is that the carrier in the output is removed by the IC221 filter and simultaneously subjected to phase and gain compensation.

In addition to the wobble servo, the ATIP decoder IC demodulates information from wobble signals such as the ATIP sync, absolute time, recommended recording power, lead-in area start time, lead-out area start time, and desk applications and sends the signals to the mechanism - control microcomputer.

To suddenly change the revolution speed of the spindle motor through start, stop, or search operations, the unit changes to CAV with the mechanism-control microcomputer. The microcomputer counts the FG signals that can be acquired from the spindle motor which enables the unit to go to the desired revolution speed in a short time due to the acquisition of the current revolution speed information.

It is necessary to control forward/reverse as the spindle driver IC (IC108 : LB1687) does not have a speed reduction function. A polarity discriminating/inverting circuit consisting of IC223 and IC224 (1/2) as shown in Fig. 5-14 is necessary because of the polarity of a normal spindle control signal is erroneous in regard to the reference voltage.

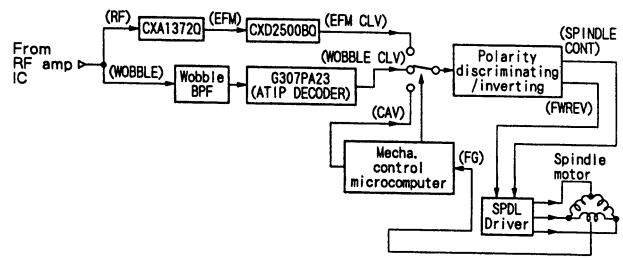


Fig. 5-13 Spindle servo block diagram

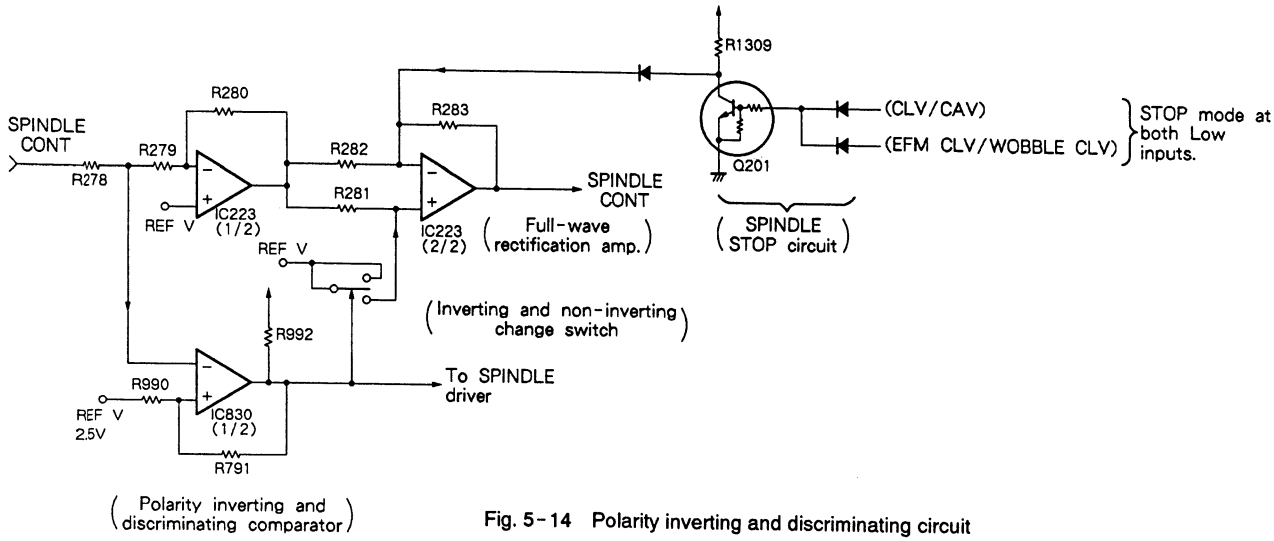


Fig. 5-14 Polarity inverting and discriminating circuit

Positive polarity increases and negative polarity decreases the speed according to the reference voltage, so the reference voltage is compared with the spindle control signal using IC224 (1/2). IC223 (2/2) becomes the inverting amp in speed decrease mode only so that the positive control signal inverts to a negative when the switch (IC217) is changed and a polarity discriminating signals are input to FRC (pin 27) in the spindle driver IC.

5.3.7 Defect Circuit

After inverting the RFI signal, the defect circuit performs bottom hold using a long and a short time constant. The bottom hold performed by the short time constant sends a response at a mirror surface defect on the disc that is 0.1 ms or longer. The bottom hold performed using the long time constant continues holding the mirror surface at the level preceding the defect. These signals are differentiated with an AC coupling and their level is shifted. A mirror-side defect signal is generated by comparing both signals. The resulting signals is used to mute a tracking error and hold the values preceding a focus and spindle error when the DEFECT output is H to improve the playability.

The circuit block diagram is shown in Fig. 5-15 and each waveform is shown in Fig. 5-16.

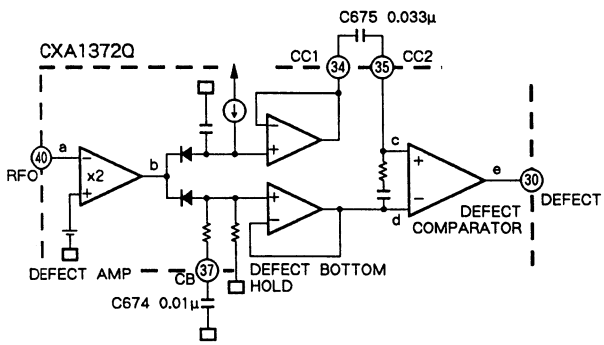


Fig. 5-15 DEFECT circuit

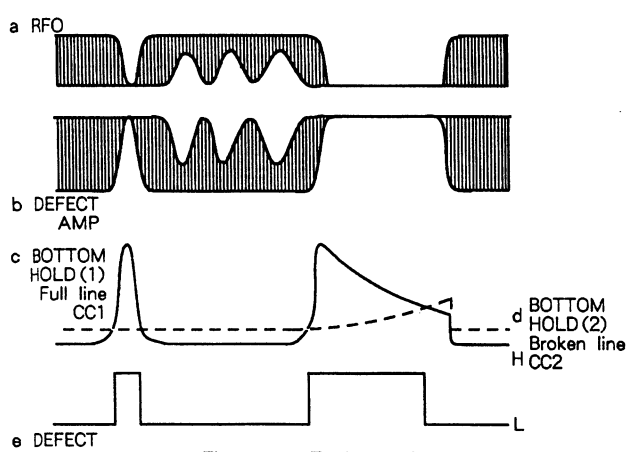


Fig. 5-16 Each waveform

5.3.8 EFM-PLL

To demodulate played EFM signals when "T" is the channel clock cycle, a channel clock signal is necessary due to modulation of the "T" integer from 3T to 11T. Actually, a PLL is necessary to playback a channel clock signal because of the non-uniform revolution of the spindle which changes the pulse width of the EFM signals.

As shown in Fig. 5-17, a portion of the EFM signals input to RF (pin 24) of the CD decoder IC (IC225: CXD2500BQ) pass through the internal buffer and are output to ASYO (pin 27). In order to correct the asymmetry of the disc, these signals then pass through the low-pass filter configured from R918, C293, R919, and C294, and are input to ASY (pin 31) as reference voltage for the EFM comparator in the CD servo control IC.

The remainder of the EFM signals are directed to the CD decoder IC inside of the PLL. There are three levels of PLLs in the IC as shown in Fig. 5-18. The PLL on the first stage is not used for varied pitch playback. The PLL on the second stage is used to create a high-frequency clock signal necessary for the PLL on the third stage. The PLL on the third stage is a digital PLL designed to playback actual channel clock signals. It maintains a capture range of ±150kHz or more under normal conditions.

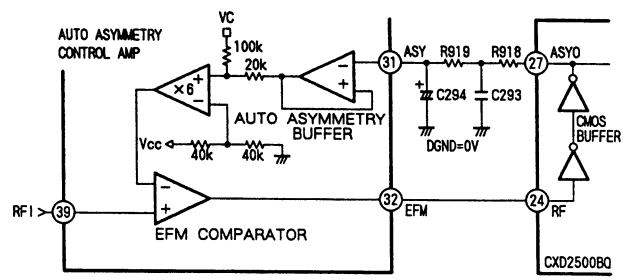


Fig. 5-17 EFM comparator circuit

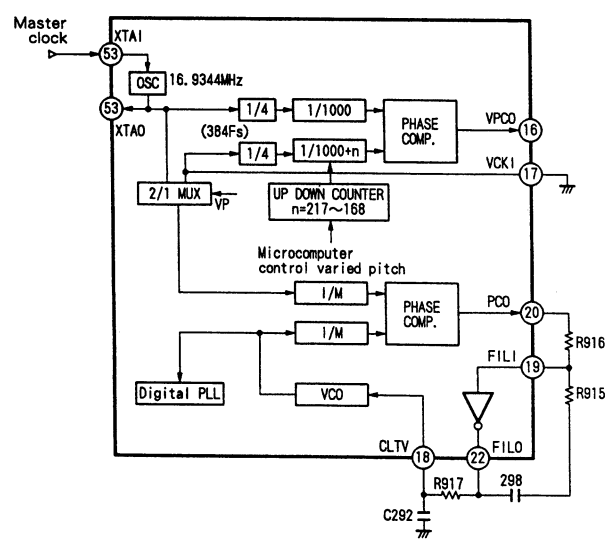


Fig. 5-18 EFM-PLL block diagram

5.3.9 RF Detection

This unit detects whether or not there are RF signals in order to determine the recorded and blank sections on a CD - R.

HF signals generated by the RF amp IC are directed to the Servo•digital board assy via CN106, and input to the peak hold circuit consisting of IC206 (1/2) and Q204 through Q207, and the bottom hold circuit consisting of IC206 (2/2) and Q209 through Q212 respectively. The two output signals pass through the differential amp [IC210 (1/2)] and are compared to the reference voltage by the comparator IC [IC207(1/2)]. The XRFDT is output to the mechanism-control microcomputer as L when an RF signal is present, and H when an RF signal is absent.

During setup, these signals are used in the TOC area to distinguish whether the disc is a TOC recording only disc (including CDs) or a disc before TOC recording. In recording mode, these signals are used for retrieval of the newly recorded area and to prevent against write-over.

The RF peak hold signals (RFT) and RF bottom-hold signals (RFB) used in OPC (optimum recording power calibration) operation are separately provided with circuits having time constants corresponding with OPC operation. Using IC213 and IC214 of the comparator and IC215 of the operation amp, the output can be acquired from the input HF signals. These detection signals are sent to the mechanism-control microcomputer.

OPC operation uses the first 4 out of the 5 bits detailed in Section 5.3.1. After recording in 15 steps, the difference of the RF peak and RF bottom signals is calculated during playback of the 4-bit section and the DA converter output level for the best possible recording is determined. During actual recording, recording with best output power is possible by selecting and supplying the output voltage closest to the set voltage using 5-bit accuracy (31-step).

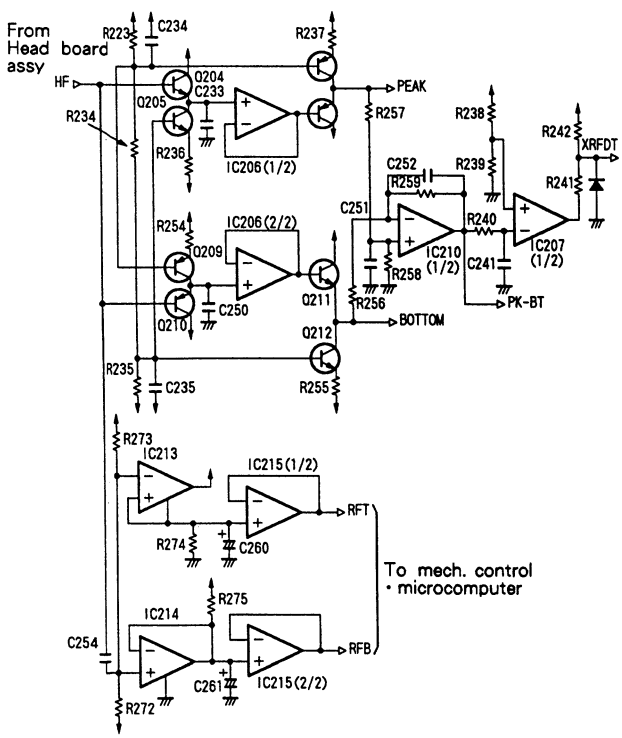


Fig. 5-19 RF detection circuit

5.3.10 Mirror Circuit

The mirror circuit block diagram is shown in Fig. 5 - 20 and the circuit diagram in Fig. 5 - 21. The mirror circuit uses a circuit unique to the CD - R and is switched with the previously mentioned RF detection signals as described below. This circuit employs RC (radial contrast) which is generated in the recorded areas by a generation circuit just as in a CD player, and in the unrecorded sections by cross-cutting the grooves on the disc.

In the blank area, peak hold signals (RC: radial contrast) acquired by the RF detection circuit are AC coupled and amplified. A mirror signal for the CD - R can then be obtained by comparing the integrated signal with a comparator [IC209 (1/2)] as reference voltage.

In the recorded area, the differential amp output of the bottom hold signal and peak hold signal used for RF detection is used. A mirror signal can then be obtained by comparing the output that has been subjected to half-wave rectifying with a comparator [IC209 (2/2)] as reference voltage.

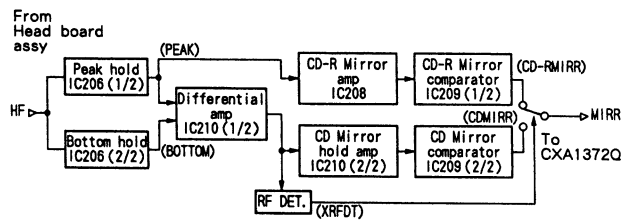


Fig. 5-20 Block diagram of Mirror circuit

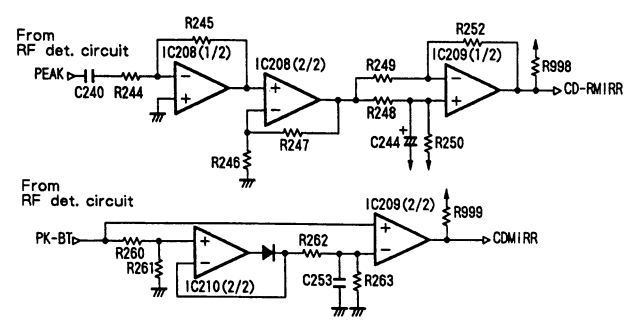


Fig. 5-21 Mirror circuit

5.4 AUDIO SECTION

5.4.1 Analog Input Circuit/Recording Volume Controls

The analog signals input from the JA802 (Lch) pin jack go through the input buffer amp (IC801) and into the VOL. board assy via CN801. These signals then pass through the recording balance volume (VR801) and recording level volume (VR802) controls and proceed into the volume amp (IC806) where they are amplified by about 20 dB. Finally they are input to the Audio board assy again via CN803.

5.4.2 AD Converter

The circuit diagram of the AD converter (IC804: CS5339) is shown in Fig. 5-22.

AINL (pin 2) and AINR (pin 27) are the analog input pins of the left and right channels respectively. ZEROL (pin 3) and ZEROR (pin 26) are the zero level input pins for offset calibration of the left and right channels respectively. Only the left channel is shown in Fig. 5-22. The 160 mV that splits 5V in the zero level input pins with R814 (1.5 k Ω) and R818 (51 Ω) is input. Signals from the VOL. board assy are biased to the 160 mV above by R810 and input to the driver amp (IC807). The driver amp output passes through the R812 and R816 resistors and into AINL of the AD converter where it is subjected to AD conversion.

The 384Fs master clock, 32Fs serial clock, and LR clock signals are input to CLK (pin 20), pin 15, and pin 14 respectively from the Servo • digital board assy via CN802 as AD converter control signals. Fs is 44.1 kHz. The 128Fs obtained by splitting the master clock signal input to CLK into three divisions is output from OCLK and input to the analog section of ICLK. The 64Fs is obtained by splitting this signal into two parts after which it becomes the sampling rate.

The AD converted data is output from SDATA (pin 16) and input to the Servo•digital board assy via CN802. The relationship between each clock and the data is shown in Fig. 5-23.

In all operation modes other than analog recording mode, APD (pin 6) and DPD (pin 10) are set to H to go to power down mode. In analog recording mode, these connectors are set to L to calibrate the analog and digital sections.

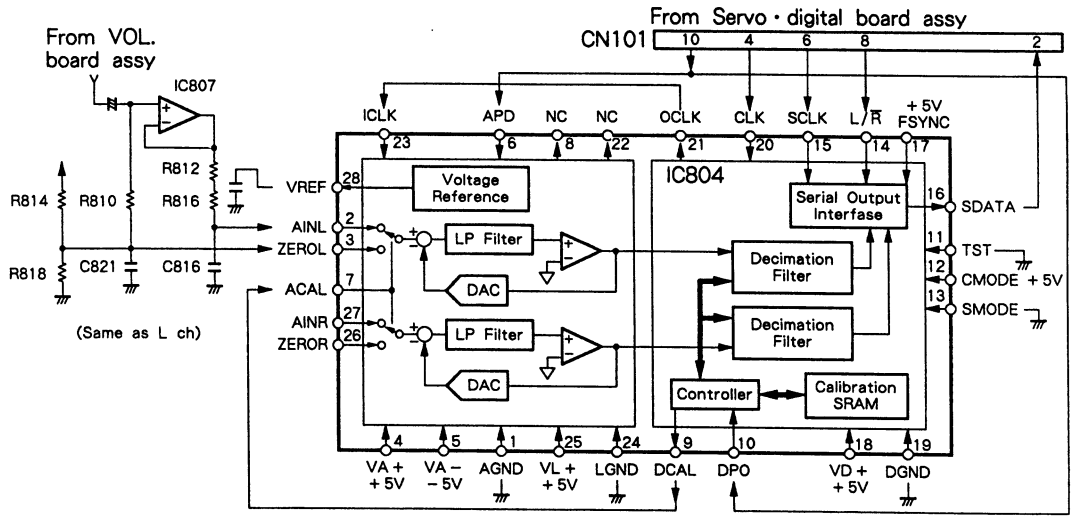


Fig. 5-22 AD converter circuit

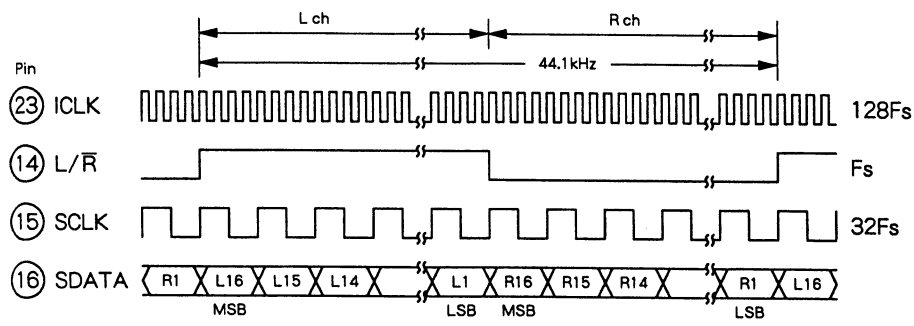


Fig. 5-23 Data output timing of AD converter

5.4.3 DA Converter

The circuit diagram of the differential amp and left channel of the DA converter (IC407: PD2029A) is shown in Fig. 5 - 24. In the DA converter, the 16-bit DATA, BCK, and LRCK are input from the Servo • digital board assy to DATA (pin 25), BCK (pin 26) and LRCK (pin 27) respectively via CN405 connector.

Also, 384Fs (Fs=48, 44.1, or 32 kHz) is input from the master clock selector to XI (pin 13) via the IC417 buffer as the master clock signal.

To set the operation mode of the DA converter, DACDT, SHIFT and LDALT serial data from the C-bit microcomputer is input from the Servo•digital board assy to MUTE (pin 22), EM2 (pin 21) and EM1 (pin 20) respectively via CN404. The contents of the data are shown in Table 5 - 1, and the serial input transfer timing is shown in Fig. 5 - 25.

This unit does not perform the attenuation and deemphasis or correspond with double speed mode. The input data is 16bit. To use the DA converter on one channel in speed mode, the IC settings are as follows: AT0 through 6 are all 1, μEM1 is 0, μEM2 is 1, HS is 0, BIT 1 and 2 are 0, MONO is 1, DFS is 0 and CHS is 0. To use the Rch (right channel) of IC408, CHS is set to 1.

The data input from DATA (pin 25) passes through the data input interface and the unnecessary noise outside of the waveband is removed by the 8-times oversampling FIR type digital filter. After the input has been filtered, the 8Fs data is directly doubled and oversampling of 16Fs is performed. Also, the dither circuit adds DC offset and dither to the data to prevent noise from the idling pattern specific to the $\Sigma\Delta$ modulation DA converter. After the dither has been added to the data, oversampling up to 384Fs is performed by the sample hold circuit.

The DA converter has built-in $\Sigma\Delta$ modulation DA converters for 2 channels (simultaneous output type). The output is bit stream output and the setup time (changing time) of the DA converters are 1/384Fs sec.

The output circuits calculate the resistance of the positive - phase output and negative-phase output that shifted the 384Fs data with the rising and falling edges of the clock signals. The phase is output from LO and $\overline{LO}$. Another channel of positive-phase output L1 and negative-phase output $\overline{L1}$ are combined with the above channels for a total of four output channels to achieve a higher signal-to-noise ratio in the DA converter output with a low distortion ratio by taking the diffential with the external operation amp (IC409). This operation amp also serves as the primary low-pass filter.

Output from the diffential amp (IC410) can be obtained also for the Rch in the same manner.

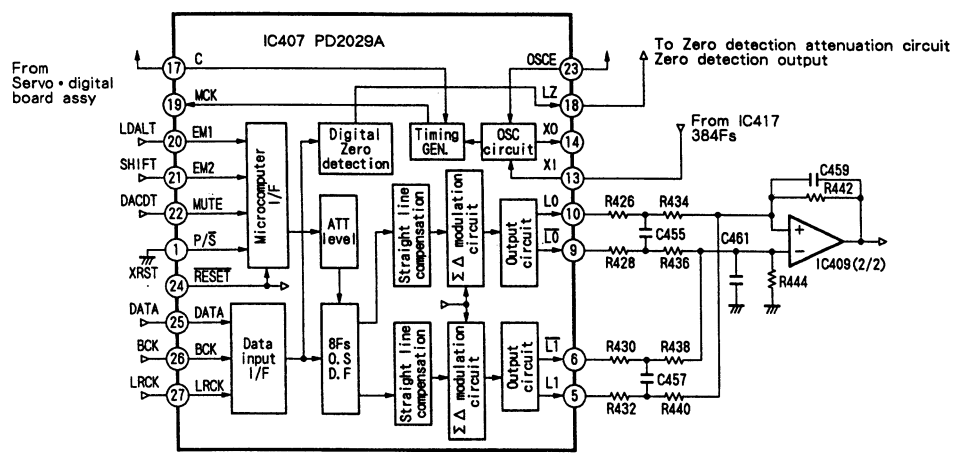


Fig. 5-24 DA converter circuit (PD2029A)

Table 5-1 Contents of serial input control

Serial input data	Control signal		
D7	0	1	
D6	AT6	0	1
D5	AT5	DFS	–
D4	AT4	CHS	–
D3	AT3	MONO	–
D2	AT2	HS	–
D1	AT1	μEM2	BIT2
D0	AT0	μEM1	BIT1

ATO – 6 :Attenuate level setting
μEM1, 2 :Deemphasis changeover setting
HS :Double speed mode setting
BIT1, 2 :Input data bit number setting
MONO :Stereo/monaural setting
CHS :L and R output selection setting at monaural
DFS :Digital filter changeover

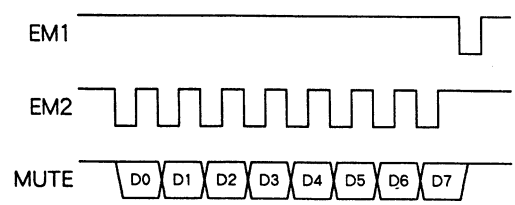


Fig. 5-25 Serial input transfer timing

5.4.4 Analog Output Circuit

The circuit diagram of the Lch output buffer is shown in Fig. 5-26. As stated above, IC409 output is input to the inverting input pin of IC409 via R446, R448 and R458. The IC409 output is connected to the FET (Q413 and Q415) buffer. This buffer makes up the secondary low-pass filter with C465, C467, R448, R458 and R456.

The analog output circuit section has the following three responsibilities.

First, it serves as the deemphasis circuit. When playing discs on which a preemphasis has been placed, the DEEMP control signal goes to H and the Q411 transistor goes to ON. At this time, the deemphasis is placed by R446, R450 and C462.

Second, this circuit serves as the muting circuit. When the POWER switch is turned ON or OFF and the input selector is switched, the MUTE control signal goes to H, the Q419 muting transistor goes to ON, and the audio output is muted.

Third, this circuit serves as the zero detection attenuation circuit. This is designed to improve the signal-to-noise ratio when all of the data input to the DA converter is 0 (when there is no input). When the DA converter does not detect any signals, the ZERO control signal goes to H, the Q471 attenuate transistor goes to ON, and the audio output noise level is reduced.

Also, the buffer output near the muting is directed to the H.P. board assy.

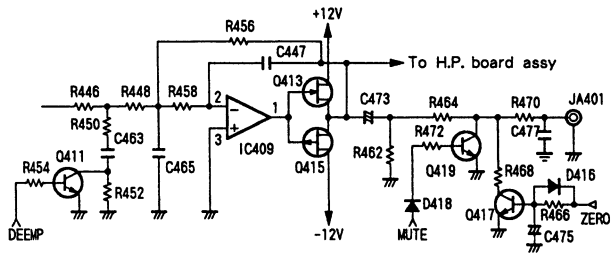


Fig. 5-26 Deemphassis, muting and zero detection attenuation circuit

5.5 Digital Audio Section

5.5.1 Digital Interface Demodulation Circuit

This unit has four systems of digital input: one coaxial (COAX) and three optical (OPT). The waveform of COAX input is shaped by the two inverters in IC302, output from pin 4 in IC302, and finally input to pin 2 of the digital interface decoder (IC301: M65810FP). OPT1, OPT2 and OPT3 input signals are converted photoelectrically using the JA302, JA301 and JA310 optical reception modules respectively, and input to pin 5, pin 6 and pin 7 of IC301. At this point, turn the power of the optical reception modules off when you wish to avoid noise during COAX input.

A block diagram of the digital interface decoder (M65810FP) is shown in Fig. 5-27. The input signals from pins 2, 5, and 6 are selected with the input changeover circuit. The preamble block detects the selected signals and generates the clock signals locked to the selected signals using VCO of the PLL circuit. The input signals are subjected to bi-phase demodulation through these clock signals, and the audio, C-bit, U-bit, and V-bit data are output. The selected signal is output from pin 1 as loop output.

The PLL is configured as follows. The output that compares the phases of the preamble and clock signals from the VCO that have been divided are output from PDO (pin 26), passed through the DC amp configured from the first inverter between pin 13 and pin 12 and the second

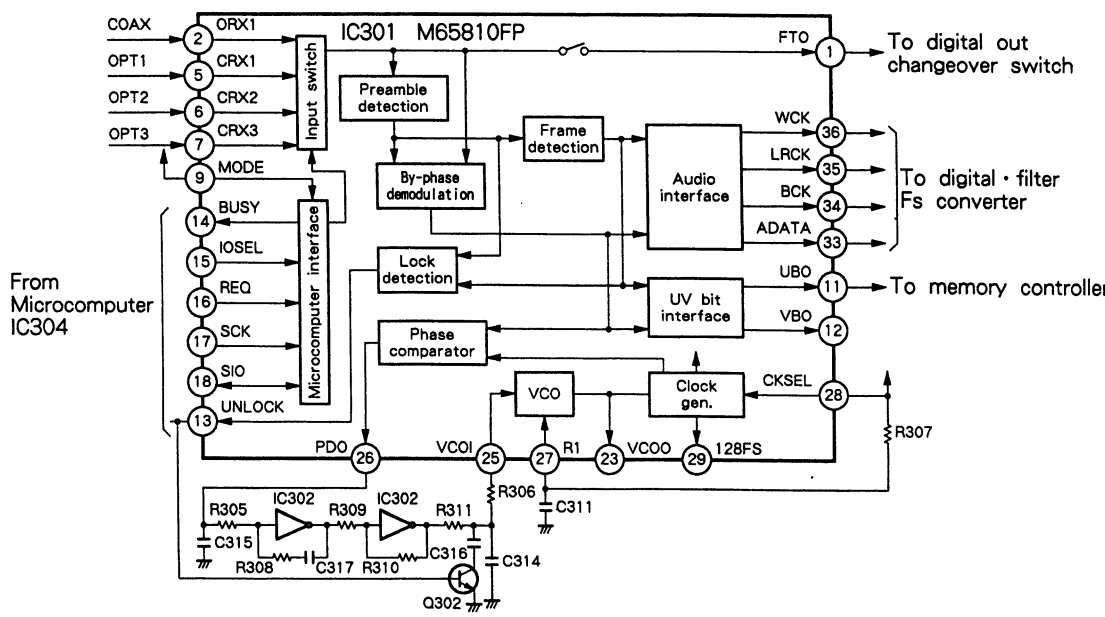


Fig. 5-27 Digital interface decoder(M65810FP)

inverter between pin 11 and 10 in IC302, and input from VCOI (pin 25) to the VCO. When the PLL is not locked, the UNLOCK signal from pin 13 goes to H and the Q302 transistor goes to ON. A pulse signal is then output to PDO and input to VCOI. As a result, the VCO sweeps between the low and high frequencies. In UNLOCK mode, the above data is not output.

The output timing of the audio data is shown in Fig. 5-28. LRCK, WCK, BCK and DATA are output from pin 35, pin 36, pin 34 and pin 33 respectively. BCK is 64fs, DATA is MSB first, binary, and 16-bit. This output is directed to the digital filter (IC312) and FS converter (IC307).

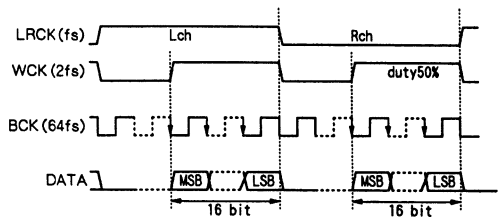


Fig. 5-28 Audio data output timing

This digital interface decoder is controlled by the C-bit microcomputer and the timing is shown in Fig. 5-29. In input mode (IOSEL: pin 15=H), SIO (pin 18) is read out at the falling edge of SCK (pin 17), and the input conversion and FTO (pin 1) control are performed with the last 4-bit data at the falling edge of REQ (pin 16).

The relationship between the data and each mode is shown in Table 5-2.

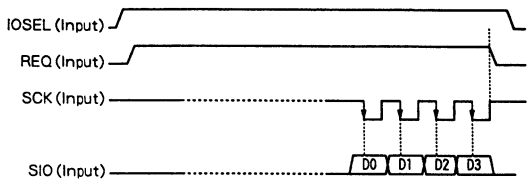


Fig. 5-29 Microcomputer control timing

Table 5-2 Data and setting mode

Receive input		D1	D2	D3
COAX	ORX1	H	H	H
(Not used)	ORX2		H	L
(Not used)	ORX3		L	H
OPT1	CRX1	L	H	H
OPT2	CRX2		H	L
OPT3	CRX3		L	H
Analog input mode		X	L	L

FTO	DO
ON	L
OFF	H

The timing that incorporates the first 32-bits of the C-bits from this IC into the C-bit microcomputer with serial data is shown in Fig. 5-30. In this figure, B of RX is the preamble shown at the front of the block. When IOSEL (pin 15) is L, SIO (pin 18) goes to output mode.

If BUSY (pin 14) is changed H in regard to the block in front of the first 32-bits of the C-bits, the signal will return to L if the contents of this block are the same as the block 2. Next, the first 32-bits in the C-bits are loaded in the register on the output side by the REQ (pin 16) reverting edge. When REQ is H, the C-bit is output from SIO follows SCK (pin 17) and input to pin 12 of the C-bit microcomputer (IC304). This unit performs readout every time transmission with the mode microcomputer is completed regardless of BUSY.

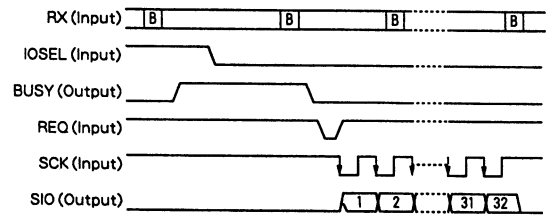


Fig. 5-30 Serial data output timing

The timing of the U-bit data output is shown in Fig. 5-31. U-bit data is output from UBO (pin 11) and input to pin 30 of the memory control IC (IC305). The figure below shows M and W of the RX reception signal as the Lch and Rch preamble respectively.

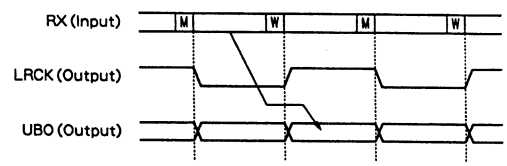


Fig. 5-31 U bit data output timing

The serial/parallel conversion circuit in the U-bit is shown in Fig. 5-32. UBO (pin 11) output of IC301 is input to pin 30 of the memory control IC (IC305). The serial/parallel conversion circuit in the IC shifts the input data in the shift register with the WCK input to pin 31. Output from the shift register is read out in the 8-bit storage register by ULAT once at 8 clocks. If the XUSEL output of the C-bit microcomputer (IC304) is L, the U-bit data in the storage register is output to pins 19 through 22 and 24 through 27, read out into pins 34 through 41 of IC304, and processed as such.

Also, the 8-bit data bus of IC304 and IC305 is a two-way bus. When the XUSEL output is H, the output from the mode microcomputer that has been converted from serial command to parallel is input as the control signal of IC305 and digital audio signal. It is then simultaneously output to pin 8 through 11 and 14 through 17 and read out in the IC305 command register at the rising edge of MLAT output (pin 32) of IC304.

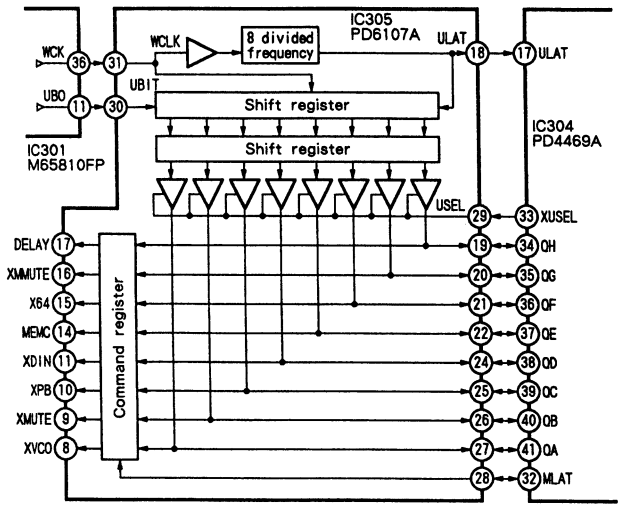


Fig. 5-32 Serial/paralle conversion circuit

5.5.2 Digital Filter

The output from the digital interface decoder is input to the digital filter and Fs converter (Fs=sampling frequency).

Refer to the section detailing the Fs converter for further information. The Fs is 32 kHz and 48 kHz due to the fact that output from this digital filter is used in sampling rate conversion mode only. DATA, BCK and LRCK are input to pin 1, pin 2 and pin 28 of the digital filter (IC312: SM5813AP) respectively and the 384 × Fs clock signal is input from VCOO (pin 23) of IC301 to XTI (pin 6) as the master clock signal.

As the digital filter output, the data from the left and right channels of the 8-times oversampling 20-bit are output from DOL (pin 24) and DOR (pin 23) respectively. The WCK and BCK synchronized with this data is output from WCKO (pin 25) and BCKO (pin 26) respectively. The timing of this output is shown in Fig. 5-33. The data and clock signals are input to the Fs converter IC (IC307) in present form and are subjected to sampling rate conversion.

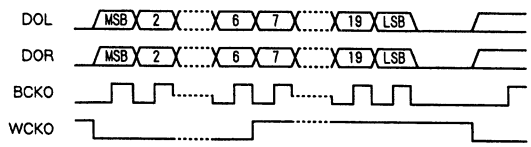


Fig. 5-33 Digital filter output timing

5.5.3 Fs Converter

The Fs converter (IC307: PD6093A) converts signals to CD format 44.1kHz digital data when the sampling frequency of the digital input is 48 or 32 kHz. To convert the data, the data sampled with 44.1 kHz is calculated from the digital filter output data that was subjected to 8-times oversampling of 48 kHz or 32 kHz.

Below is an explanation of the actual circuit as shown in Fig. 5-34. First, the output data from the digital interface decoder is input to EXDI (pin 37), EXBI (pin 38), EXWI (pin 39) and EXLI (pin 40). One portion of the data from the digital filter is input to BCK8F (pin 116), WCK8F (pin 117), L8FSI (pin 118) and R8FSI (pin 119). When the sampling frequency is 44.1 kHz, TRD (pin 96) goes to L and OSEL (pin 97) goes to H via FSC (output changeover of Fs converter) and the XFEN control signal output from the C-bit microcomputer (Fs converter is enabled with L). At this point, the signals input to pin 37, pin 38, pin 39 and pin 40 are output from DATAO (pin 32), XOUTCKO (pin 34), WCKO (pin 35) and LRCK44 (pin 36) respectively.

When the sampling frequency is any frequency other than 44.1 kHz, TRD is L and OSEL is H and the PLL (IC308) goes to ON. The VCO output from IC308 is output from VCO (pin 4) and input to MCKI (pin 112) of IC307. The signals split into 294 divisions (Fs=48kHz) or 441 divisions (Fs=32 kHz) are output to COMPO (pin 3). The I3248 (pin 98) performs switching between the two frequencies via FS32 control signals (H when Fs=32 kHz) from the C-bit microcomputer. The signals obtained by splitting WCK8F are output from REFO (pin 2). The COMPO and REFO signals are input to COMPI (pin 3) and SIGI (pin 14) of IC308, and the phase comparison signal is output from PC20 (pin 13). This PC20 is input to VCOIN (pin 9) through a filter. As a result, the VCO oscillates with the 14.112 MHz locked to either 32 kHz or 48 kHz and is used by IC307 as the sampling rate conversion clock signal.

The data read out from L8FSI and R8FSI is used to perform the serial/parallel conversion with the shift register. It is converted into the Fs=44.1kHz data by performing calculations with the coefficient ROM data, and then output to XOUTCKO, WCK440, LRCK44 and DATAO which were created by the timing generation circuit. The output signals are then input to the jitter absorption buffer (IC315). The operation waveform of the PLL is shown in Fig. 5-35.

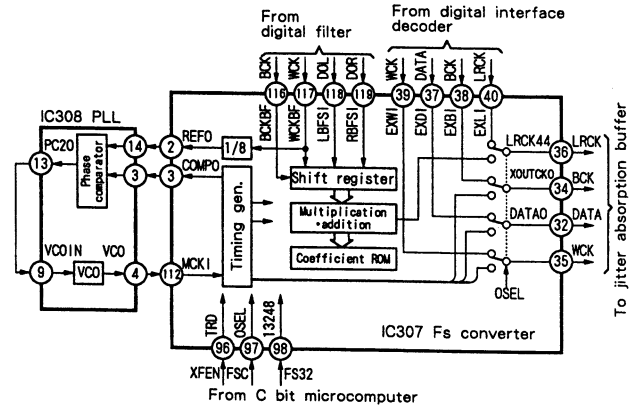


Fig. 5-34 Periphery block diagram of Fs converter

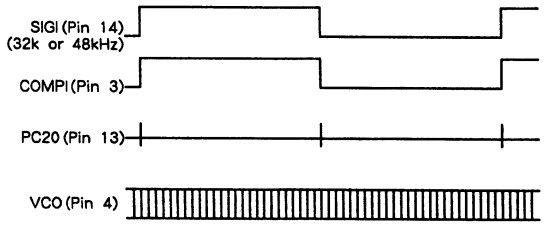


Fig. 5-35 PLL(IC308) operating waveform

5.5.4 Jitter absorption data buffer

In this IC, the digital interface decoder data and clock signals from the Fs converter as well as FS converted data and clock signals have jitter. As a result, another trigger is placed on the signals using jitter-free signals made by the VCO and clean clock signals and data are supplied to the other circuits.

The following is an explanation of this circuit based on Fig. 5-36. FS converter output is input to LRCK1 (pin 4), WDCKI (pin 3), BCK1 (pin 6), and DATAI (pin 9). The 16.9344 MHz output from VOUT (pin 8) of PCX1021 (IC316) of the VCO is input to VCOI (pin 20) of IC315. This output is divided to create LRCK and LRCK1 which are used in performing the phase comparison. If the difference in the phases of the two LRCK is 90- or more, the output will be distinguished as analog output and the mute function will be enabled. The phase comparison signal is output from PD (pin 18) through the IC317 filter, input to VIN (pin 1) of VCO, and the oscillation frequency is controlled.

Input from the Fs converter, that has had another trigger applied to it with a VCO clock signal, is output to LRCK2 (pin 28), WDCK2 (pin 27), BCK2 (pin 25) and DATAO (pin 1) and directed to the memory control IC (IC305).

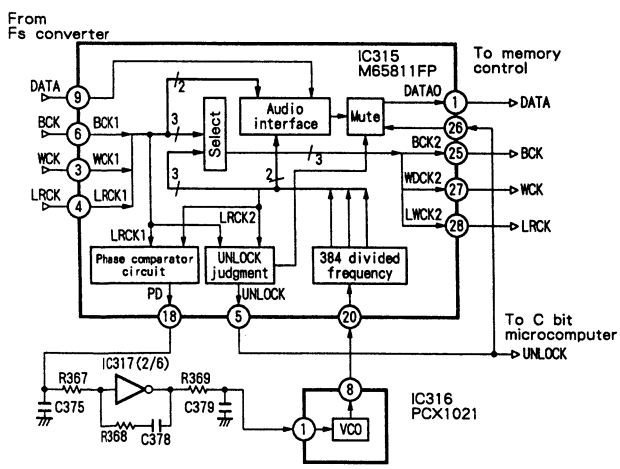


Fig. 5-36 Jitter absorption data buffer circuit

5.5.5 Memory controller

The memory controller (IC305: PD6107A), in addition to the functions mentioned in 5.5.1, has audio data, clock selector, digital mute and a function for recording audio data delay.

The following is an explanation based on Fig. 5-37. First, the data selected with the selector by combining XPB (pin 10) and XDIN (pin 11) received from the C-bit microcomputer is output to SDATA (pin 3), SBCK (pin 1), SWCK (pin 80) and SLRCK (pin 79).

In playback and stop modes, XPB goes to L and the signal from the CD decoder IC (IC225) input to PDATA (pin 69), PBCK (pin 70), PWCK (pin 71) and PLRCK (pin 72) is selected. When there is digital input in recording mode, XPB goes to H, XDIN goes to L, and the signal from the jitter absorption buffer input to DDATA (pin 74), DBCK (pin 75), DWCK (pin 76) and DLRCK (pin 77) is selected. When there is analog input in recording mode, both XPB and XDIN go to H and the AD converter signal input to ADATA (pin 64), ABCK (pin 65), AWCK (pin 66) and ALRCK (pin 67) is selected.

Each selected clock signal is input to the DA converter (IC), level meter interface (IC320), digital fader (IC309) and EFM encoder (IC311), and the data is input to the level meter interface and digital fader.

The digital fader output is input from FDATA (pin 6) again, passed through the mute circuit which activates with one word as distinction from the C-bit microcomputer, output to MDATA (pin 5), and finally directed to the DA converter.

The signals that pass through the mute circuit are sent to the memory control section in recording mode only.

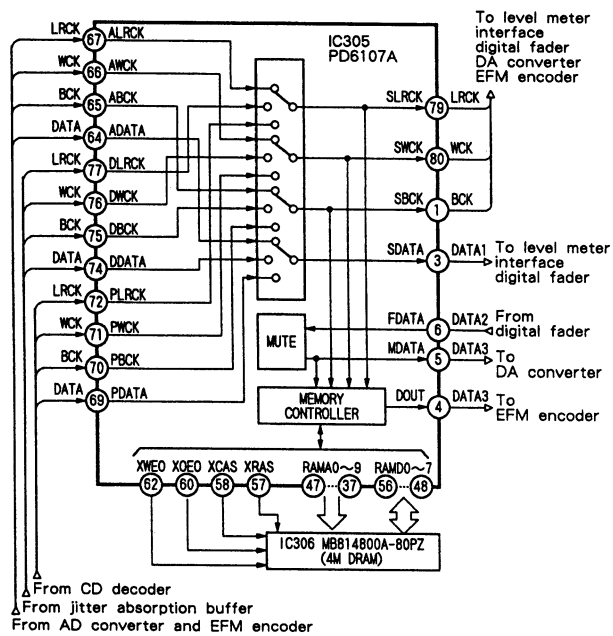


Fig. 5-37 Periphery block diagram of memory controller

The 16-bit data that is split into 8 bits, subjected to serial/parallel conversion every 8 bits, and sequentially written in the 4 Mbit DRAM. After about 3 seconds, the data is read, subjected to parallel/serial conversion, output to DOUT (pin 4), and directed to the EFM encoder.

5.5.6 Digital Fader and Level Meter Interface

The memory controller selector output is input to the digital fader (IC309: PD0026A). WCK, DATA and BCK are input to WCLK (pin 13), DATA (pin 14) and BCLK (pin 15) of IC309 respectively and the attenuation data is output to DOUT (pin 4).

The attenuation level is determined from the 8-bit data input to ADATA (pin 6) from the mode microcomputer (IC701: PD4468D) of the Function board assy.

The block diagram of the digital fader is shown in Fig. 5-38.

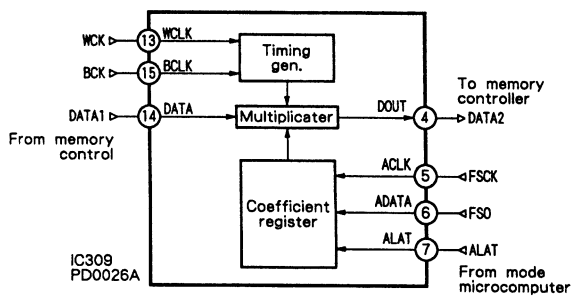


Fig. 5-38 Digital fader block diagram

The level meter interface (IC320: PD2020) output is identical to the memory controller selector output. It is input to LRCK (pin 34), WCK (pin 35), BCK (pin 36) and ADIN (pin 41). Absolute value and logarithmic conversions are performed on the data, which are read from SDATA (pin 15) as peak hold 8-bit data. The level meter on the front panel will then light.

This output is controlled from the mode microcomputer in the Function board assy through LR (pin 12), XRD (pin 13), FSCK (pin 14) and XSOE (pin 16). LR is the channel setting (Lch is H). XRD sends the peak hold data with L to the shift register of the CPU I/F and clears the peak hold as well. XSOE is H and SDATA is Hi-Z. When XSOE is L, the data is output following the XSCK serial clock signal.

The block diagram of the level meter interface is shown in Fig. 5-39.

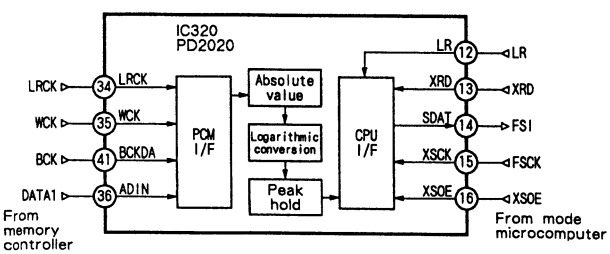


Fig. 5-39 Digital fader block diagram

5.5.7 EFM encoder

The block diagram of the EFM encoder (IC311: LC89583) is shown in Fig. 5-40. The clock and delayed data selected with the memory controller is input from DBC (pin 31), DLRC (pin 30) and DIN (pin 29) of the EFM encoder. This IC also has another audio interface. The LR clock signals are used with output as AD converter clock signals, however in recording mode the input is for the laser power calibration. By inputting the EFM output, calibration is performed using random data.

First, the input data passes through the MUTE circuit controlled from the mechanism-control microcomputer. For the output from the MUTE circuit, the interleave operation is performed in the CIRC (Cross Interleave Read - Solomon Code) encoder, C1 and C2 correction bits are added, and EFM modulation (Eight to Fourteen Modulation) is performed at the same time as the subcode, sync and merge bits are added. The output signals finally become CD format EFM signals after they have been subjected to NRZI conversion.

The signal on the disc is a signal from 3T to 11T (t=231 nsec). To create the ideal pit length in playback mode, slightly shorten the time that the LD (laser diode) is ON. More specifically, the 3T through 11T pulses go to N - 1T and are set to 2T to 10T. Only 2T is converted into a long 60 nsec pulse. These signals are output from EFM (pin 23) and proceed through the EFM control buffer (IC319: TC7S08F) via CN201. The signals then go through the LD drive circuit in the Head board assy and are input to the pickup of the LD where each signal is recorded.

There is a PLL that generates EFM system master clock (IC310: MC74HC4046AN) in the area of the EFM encoder. The 44.1 kHz divided from the master clock (16.9344 MHz) signals input from DCK (pin 32) of the EFM encoder, are output from PC1 (pin 95) and input to SIGI (pin 14) as the reference signals for the phase comparator of the PLL. The VCO output (pin 4) of the PLL is input to VCOIN (pin 96) of the EFM encoder and used as the EFM system master clock (8.6436 MHz).

The 196 - division clock signals are output from PC2 (pin 100), there phases compared with the phase of the above signals, and input from COMPI (pin 3) of the PLL as phase comparison signals. The phase comparator signals are output from PC20 (pin 13) and input to VCOIN (pin 9) as VCO control voltage. For SRAM (IC318: HM6264ALFP-12T) connected as the CIRC encoder, XMRD (pin 79) and XMWR (pin 80) are output as the control signals, and MAD0 (pin 65) through MAD11 (pin 76) are output as address signals. The data is input and output by MD0 (pin 81) through MD7 (pin 88).

An ATIP sync is input from the mechanism-control microcomputer to ATIPSYNC (pin 47) in order to synchronize the sub-code sync of the EFM signal to be recorded and ATIP sync on the disc. Sync operation is enabled when XEXTSYC (pin 49) goes to L.

Synchronization is performed in recording standby mode. The sub-code sync of the EFM signal is output from SUBSYNC (pin 2) for confirmation and read out into the mechanism-control microcomputer.

ENCE, MSCK and MSO are input from CE (pin 59), CL (pin 60) and DI (pin 61) respectively from the mechanism - control microcomputer as control signals. The control signals are effective when CE is H and DI data is read out at the CL rising edge. This is used for setting the operation mode of the EFM encoder and inputting subcode P and subcode Q.

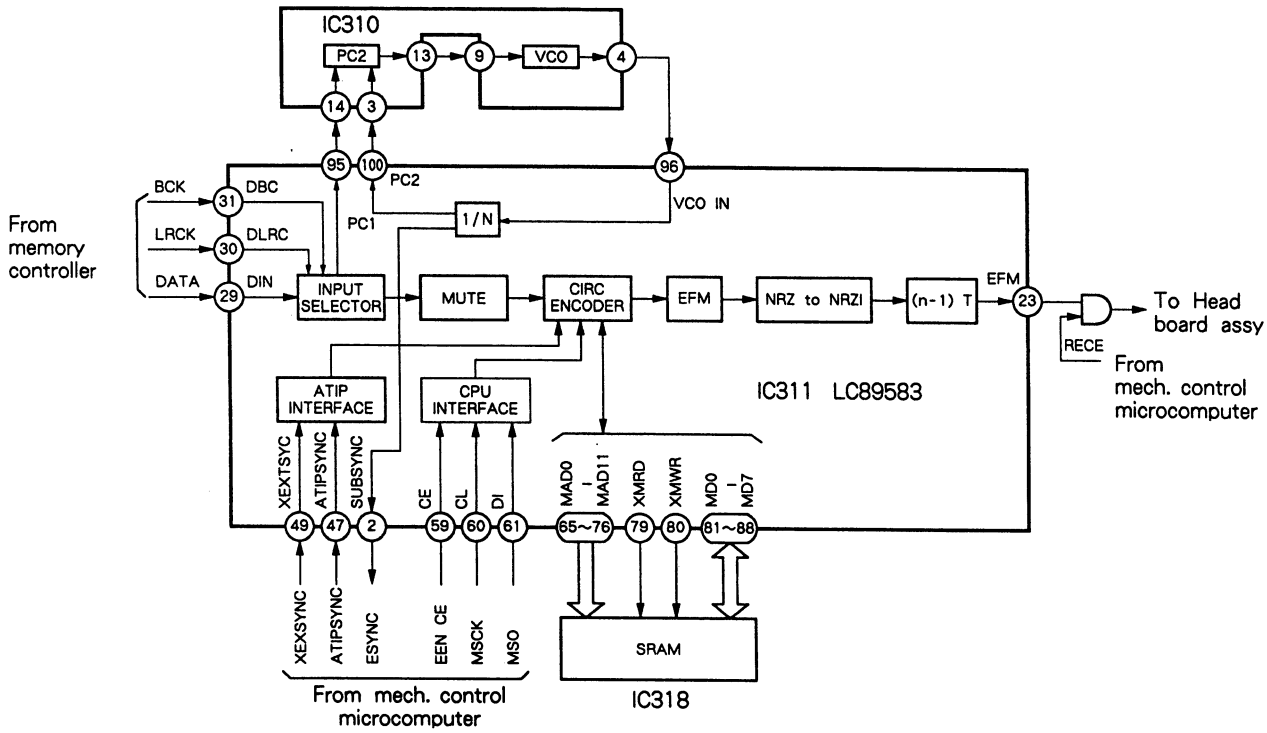


Fig. 5-40 Periphery block diagram of EFM encoder

5.5.8 Digital Audio Output

In the digital audio output, an analog input signal or signal encoded by the CD decoder (IC225: CXD2500BQ) and loop signal from the digital input or playback signal from the disc are subjected to AD conversion. The signals encoded by the digital interface encoder (IC321: TC923 1N) are selected by the selector (IC322: TC74HC153AP) and output from the coaxial (JA305) or optical (JA304 and JA311) output.

The DATA from the AD converter (IC804: CS5339) and LRCK and BCK made by the EFM encoder is input to the digital interface encoder. The C-bits are output with the category set to CD, the sampling frequency at 44.1 kHz, no emphasis, copy prohibited and the clock accuracy at ± 1000 ppm. The block diagram of the digital audio output is shown in Fig. 5-41.

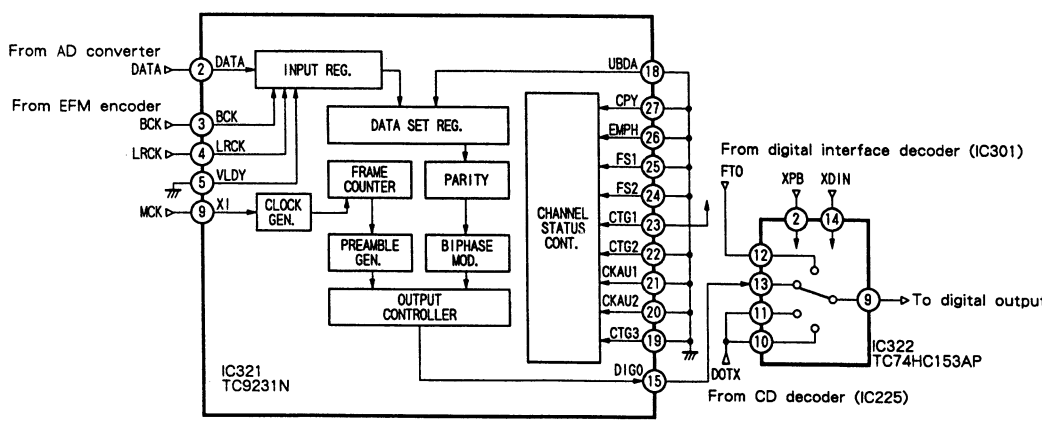


Fig. 5-41 Periphery block diagram of digital audio output

5.5.9 C - Bit Microcomputer

The C-bit microcomputer (IC304: PD4469A) controls the operation mode of the digital emphasis decoder, decodes the C and U-bits, performs transmission with the mode microcomputer, and converts serial commands from the mode microcomputer into parallel. Refer to the description on PD4469A in "7. IC Information" for further details about the output.

5.5.10 Master Clock System

The circuit diagram of the master clock system is shown in Fig. 5 - 42. In recording mode when the Fs is 48 kHz, the 384-times clock signal of the Fs is output with digital input from VCOO (pin 23) of the digital interface decoder. These clock signals are input to XTI (pin 6) as the master clock signals for the digital filter where 8-times WCK of the Fs is output to WCKO (pin 25). The 8 Fs clock signals are input to WCK8F (pin 117) of the Fs converter and 8 - division signals are output from REFO (pin 2) as PLL reference signals. They are then input to SIGI (pin 14) in the PLL and make a 294-times clock signal (14.112 MHz). This signal is output from VCO (pin 4), input from MCKI (pin 112) as the Fs converter master clock, and subjected to a sampling frequency conversion. At this time, the master clock signal from LRCK44 (pin 36) is split into 320 divisions and 44.1 kHz is output. It is then input to the jitter absorption buffer from LRCK1 (pin 4) as a reference clock signal. It consists of a VCO lithium rate and double PLL. This VCO oscillates on 384-times 16.9344 MHz of 44.1 kHz. The VCO clock signal serves as the master clock signal during digital output except for the clock input to pins 5, 6, 10 and 12 of IC 314.

When the Fs digital input is 32 kHz, the REFO output is 32 kHz. In this case, the divider in the Fs converter changes but the frequency of the Fs converter master clock does not change. Like before, 44.1 kHz is output from LRCK 44 and serves as the reference for the jitter absorption buffer.

In recording and playback modes during analog input, 16.9344 MHz of the crystal oscillator in the Audio board assy serves as the master clock signal of this system and is input to pin 3, 4, 11 and 13 of IC314. The oscillation of VCO of digital interface decoder and jitter absorption buffer are stopped at this time.

Two or more 16.9344 MHz master clock signals are matched to the operation mode and selected by IC314. The output from pin 7 by the master clock selected here is directed to the EFM encoder and CD decoder, and serves as the reference of the servo system. The output from pin 9 is directed to the digital interface encoder and DA converter in the Audio board assy to avoid control from the input select on the front panel when recording PMA and PCA.

In the Audio board assy, the selected master clock signal is also used via IC419 in order to improve the audio quality.

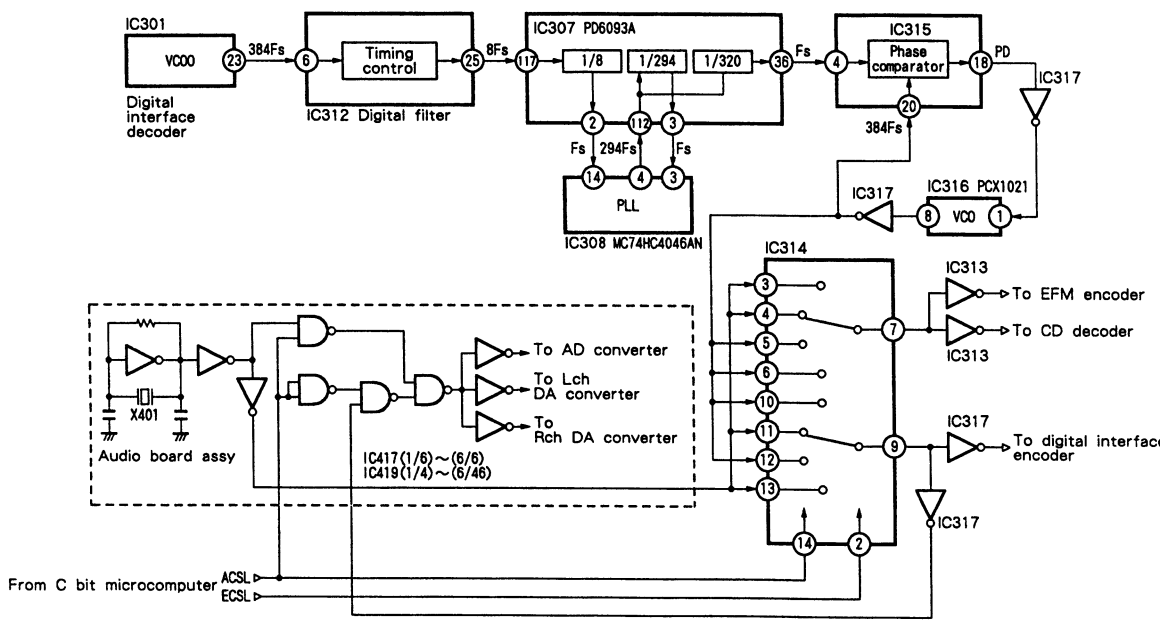


Fig. 5-42 Master clock circuit

6. ERROR DISPLAY AND TROUBLESHOOTING (MICROCOMPUTER)

6.1 ERROR CODES

When an error is detected, the corresponding code appears on the FL display of this unit. Operation will be stopped when it cannot be continued. Press the operation keys (including keys on the remote control unit) to clear the displayed error and return to the normal display.

Error codes are displayed with 7 segment digits on the FL display (TRACK to SEC) as follows.

When an error occurs

First, the error is displayed with Err xx and two digits in the minute display position. To provide for easy use, the errors are numbered and appear on the display as shown in Table 6 - 1. When these error codes are displayed, press the SKIP ON/OFF button to check the details of the errors for servicing. Each time you press the SKIP ON/OFF button, the display changes between the service error and user error display.

Table 6-1

Error No.	Error	Instructions
00	Hardware error HErr 00:00, 01:xx 02:xx, 03:xx Err xx:80, xx:81 xx:8F,	Turn the power off and on again. If the same error persists, contact service personnel.
01	Expired the battery HErr 00:BA	The life of the built-in lithium battery has expired. Contact service personnel to change the battery.
02	Mech. lock error Err xx:19	Internal mechanism does not work. Check the lock and spacer for transport.
03	Loading error Err 01:31, xx32 Clamp-up error Err xx:46	Error in loading section. Hold the tray by hand and check for loose or stuck parts.
04	Disc distinction error Err xx:20, xx:34 xx:82, xx:A4 xx:43, xx:86 xx:88	Error with set disc. The disc is inserted wrong-side up or the disc is dirty or scratched.
05	Recording error Err xx:37, xx:38 xx:83, xx:87 xx:88, xx:90 xx:A5	Recording is not possible. Check if the disc is dirty or scratched.
06	Recording stop error Err xx:84, xx:85 xx:A6	Recording stops due to scratches or sudden shock to the disc. Check if the disc is dirty or scratched. Do not shake the unit during recording.
07	TOC write error Err xx:39, xx:40 xx:A7	Error in TOC write. Some recorded discs cannot be played by CD player.
08	Disc open error Err xx:41, xx:A8	Information-write error on the disc when ejecting the disc. Press the OPEN/CLOSE button again. The tray will open without recording any information on the disc if 16 attempts are made without success. Check for dirtying or scratches on the disc.
09	Other errors	Check for dirtying or scratches on the disc. Contact service personnel if the same error still occurs.

The service-use error codes are as follows.

TRACK INDEX MIN SEC TRACK INDEX MIN SEC

E rr XX YY or HE rr XX YY

XX and YY indicate the mode when an error occurs and the error code using numbers 00 to 99.

6.2 EXPLANATION OF SERVICE ERRORS

6.2.1 Errors When Power is Turned ON

When you turn the power ON, the mechanism-control (UPD78323GJ-5BJ) and mode-control (PD4468D) microcomputers go to self-check mode. If an error is detected, the corresponding error code is displayed, and operation is stopped.

For errors which are detected when the power is turned ON, HE rr XX YY is displayed distinguishing from the error display during normal operation.

The following error explanation enumerates the possible damage.

XX = 00 : Errors detected by the mode-control microcomputer and can be classified into the following two types depending on the YY value.

YY = 00 : Error in transmission with the mechanism - control microcomputer.

If transmission with the mechanism-control microcomputer fails while the main routine is performed 256 times (about 8 seconds) after turning the power on, an error code is displayed and the operation is hung up.

The cause of this error is a defective connector, or insufficient power supply to the Servo•digital board assy.

YY = ba : Mechanism-control microcomputer check sum (battery) error

Occurs when damage to the backup RAM in the Servo • digital board assy is detected. When this error occurs, this unit will prohibits all recording.

This is because recording operation is protected against power outage by the backup RAM. An error occurs when this function does not function correctly.

The possible causes are that the life of the lithium battery in the Servo • digital board assy has expired, an inferior power system, or defects adjacent to the RAM section.

XX = 01 : Mechanism-control microcomputer PORT check error

When a self-check of the mechanism-control microcomputer is performed, the control pins are checked. If an error occurs, the pin number of the problem pin appears and the operation is hung up.

HE rr 01 ◯◯ → Pin no. of problem pin appears.

XX = 02 : Mechanism-control microcomputer ROM error

This error occurs and the operation is hung up if an error is detected in the area of the mechanism-control microcomputer expansion ROM.

The possible causes are defects in the ROM itself or in circuits adjacent to the ROM in the Servo•digital board assy.

XX = 03 : mechanism-control microcomputer RAM error

This error occurs and the operation is hung up if an error occurs in RAM write when self-checking the RAM of the Servo•digital board assembly.

The possible causes are defects in RAM itself or in circuits adjacent to the RAM in the Servo•digital board assy.

6.2.2 Errors During Normal Operation Part 1 (YY<80)

When an error occurs during normal operation, E rr XX YY appears and operations are stopped when they cannot continue.

The numbers for XX show the mode when the error occurs and that sent to the mechanism-control microcomputer from the mode-control microcomputer, as follows.

XX = ?0 : Unknown
- ?1 : OPEN
- ?2 : CLOSE/STOP
- ?3 : SET UP (disc loading)
- ?4 : TOC READ (including SET UP)
- ?5 : PLAY
- ?6 : SEARCH
- ?7 : REC/PAUSE
- ?8 : REC
- ?9 : END REC (lead-out recording during TOC WRITE)
- ?A : TOC REC (lead-in recording during TOC WRITE)
- ?B : PMA REC (temporary TOC information recording)
- ?C : OPC (power calibration)
- ?D : TOC CHECK (restoration of error disc)
- ?E : No function
- ?F : Recovery operation from power isolation

Note : ? represents a number from 0 to 9.

YY is a display of an error code detected by the mechanism-control microcomputer.

YY = 2 : STOP operation (cannot check if the spindle motor has stopped.)
- 4 : Focus operation (focus cannot be aligned)
- 5 : Spindle motor is not CAV locked.
- 6 : After tracking closes, a CAV lock cannot be checked within 10 seconds.
  - With CD : Subcode cannot be read within 10 seconds.
  - With CD - R : ATIP information cannot be read within 10 seconds.
- 7 : 1 track jump (outer direction)
- 8 : 1 track jump (inner direction)
- 15 : Track count search (outer direction)
  - 1 search is not finished within 3 seconds.
- 16 : Track count search (inner direction)
  - 1 search is not finished within 3 seconds.
- 17 : PAUSE
  - The current position is lost for 3 seconds or more during pause (ATIP/sub-code cannot be read.)
  - Synchronization of the encoder does not succeed for 3 seconds.
  - Does not return to original position after shock during play.
- 18 : PLAY ····· PLAY cannot continue.
- 19 : SEEK TRACK0
  - SSTOP signal is not generated within 3 seconds when the pickup returns to the original position.
  - TOCPOS signal is not generated within 300 ms.
- 20 : BLANK SEARCH
  - The current position is unclear for 3 seconds or more. (ATIP/sub-code cannot be read.)
- 21 : At the beginning of recording
  - Write-over is not possible due to a problem with the write-over position. (causing double write)

  During recording
  - Synchronization of the encoder is released for at least 1 second and there is no synchronization.
- 23 : ATIP search
- 24 : Sub-code search (TIME)
- 25 : Sub-code search (TNO)

  } Current position unclear for 3 seconds or more, jump error, or time-out for 3 minutes 30 seconds.
- 26 : N track jump (outer direction)
- 27 : N track jump (inner direction)
- 30 : TOC area search
  - Current position unclear or bad search
- 31 : Tray open operation
- 32 : Tray close, clamp or STOP operation

33 : Setup ····· Tracking not performed after checking the disc presence.
34 : Error during TOC read
35 : Error during PLAY
41 : PMA recording area does not exist (disc full).
42 : Tracking released at least three times or search failed during OPC operation.
43 : Error not detected after TOC check.
52 : Correct read of PMA information read cannot be done. (There is an RF but the sub-code cannot be read.)
54 : The information recording position search fails (recording area on CD - R will be searched).
55 : Repeated 1 track jump (outer direction) ·····1 track jump failed.
56 : Repeated 1 track jump (inner direction) ·····1 track jump failed.
58 : Tracking released during recording power sweep in OPC operation mode.
61 : Measurement of line velocity and tracking pitch failed.(search cannot be performed)
62 : 1 track jump (auto sequence: outer direction) failed.
63 : 1 track jump (auto sequence: inner direction) failed.
64 : 1 track jump repeated (auto sequence: outer direction) ·····1 track jump failed.
65 : 1 track jump repeated (auto sequence: inner direction) ·····1 track jump failed.
66 : 10 track jump (auto sequence: outer direction) failed.
67 : 10 track jump (auto sequence: inner direction) failed.
68 : 10 track jump (auto sequence: outer direction) failed.(during manual search.)
69 : 10 track jump (auto sequence: inner direction) failed.(during manual search.)
70 : 50 track jump (auto sequence: outer direction) failed.
71 : 50 track jump (auto sequence: inner direction) failed.
72 : 50 track jump (auto sequence: outer direction) failed.(during manual search.)
73: 50 track jump (auto sequence: inner direction) failed.(during manual search.)
74 : N track jump (auto sequence: outer direction) failed.
75 : N track jump (auto sequence: inner direction) failed.
76 : After a power outage, processing to maintain REC mode failed.
77 : Surface inspection failed.
78 : Blank (gap) search in the vicinity of the specified REC. area and specified starting address failed.
79 : Return operation for "needle jump" and "focus aberration" failed during REC.

Note : The numbers not defined above are not used or error codes that do not occur.

6.2.3 Errors during normal operation Part 2 (YY>80)

When an error occurs in normal operation mode, E rr XX YY appears on the display and the unit stops when operation cannot continue.
The error codes with a YY of 80 or higher do not have any special meaning with XX.

YY = 80 : Transmission error with mechanism-control microcomputer.
This error occurs if transmission with the mechanism-control microcomputer does not succeed in at least 8 seconds. This error occurs when the power is cut or when the power switch is hastily pressed (turned from ON to OFF to ON in a short period).

81 : DIO microcomputer (PD4469A) transmission error
This error occurs when transmission between the mode-control microcomputer and DIO microcomputer does not succeed for 4 seconds or more.

82 : This error occurs when there is a disc in the unit when the power is turned on, but the contents are not known.
This error mainly occurs in the program, meaning that it is unlikely that there is a problem in the hardware.

83 : This error occurs when an abnormality exists at the place of write on the disk in REC/PAUSE mode.
This error always occurs when the unit is operated in record protect mode.
Also, this error may occur if there is dust or scratches on the disc.
It also occurs due to a problem of the unit such as when the laser diode cannot obtain recording power or the RF detection circuit is inferior.

84 : Occurs when tracking is disengaged during recording.
The cause of this error is probably a dirty or scratched disc or shock to the unit.

85 : Occurs when synchronization of the sync is disengaged during recording.
There is a problem with the digital input signals or the disc is inferior. It also occurs due to a problem with the unit such as when the clock of each PLL circuit is disengaged.

86 : TOC READ error
TOC information (including temporary TOC) was not completely prepared during disc read.

87 : When start of recording was initiated, recording didn't start within 3 seconds.
This error occurs when the FS information is incorrectly used with professional-use equipment digitally connected.

88 : This error occurs when recording is attempted and there is a problem on a disc whose recording information is abnormal. Disc needs to check.

8F : Error indicated when the mode-control microcomputer runs wildly.

90 : This error occurs when input of the skip information is attempted on a disc on which recording is not possible (problem disc).

A4 to A8 : This error occurs when the aim operation is not finished within a certain time.

6.3 EXPLANATION AND ITEMS OF CAUTION OF NEW FUNCTIONS

6.3.1 Automatic REC/PAUSE

This function controls the start/stop of recording in synchronization with playback equipment when dubbing a CD. This function uses the sub-code that is sent on the digital interface of the playback equipment.

The subcode signal separated from the digital input signal is decoded by the DIO microcomputer. If there is normal input (playback equipment is playing or "the disc is spinning"), this unit starts recording operation.

The automatic REC/PAUSE function should be used with caution based on prudent operation following the directions in the operating instructions.

Also, you should note that there are some models even of the user-type which do not output subcodes.

6.3.2 Auto Track No. Increments

When there are subcodes just as with the aforementioned functions, the subcode signal is used and precise track detection is performed. Depending on the connected equipment, there will be normal no-audio status causing erroneous operation.

6.3.3 SKIP Function

The SKIP function is defined by the format (orange book) of the CD - R. The skip information recorded on the disc does not correspond with existing CD players.

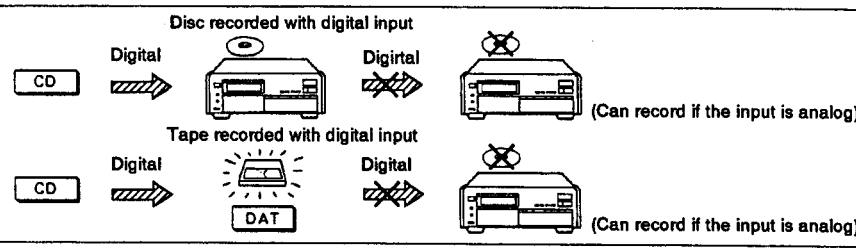
If TOC WRITE is performed using a recorder on a partial disc on which SKIP information has been recorded with this unit which does not correspond to SKIP, the SKIP information may be erased without registering this data.

6.3.4 SCMS Function

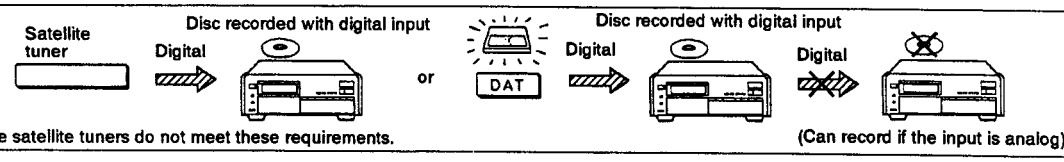
SCMS is an additional function to prohibit unregulated recording by adding information concerning copy prohibit to the digital signals. SCMS is the abbreviation for Serial Copy Management System.

This system was basically considered so that an original source (CD, etc.) can be digitally copied once. When the source is digitally copied, theoretically, there is not a loss in sound quality.

1 Copyrighted CD and DAT tapes can be digitally recorded only onto one machine.

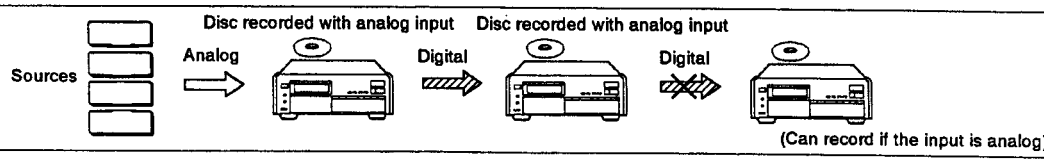


2 Digital signals from satellite broadcasts ca be digitally recorded only onto one machine.



• Some satellite tuners do not meet these requirements.

3 A disc recorded with analog input can record onto one machine regardless of the source to be recorded.



• Operation and display when recording

If it is determined through the SCMS function that recording is impossible during recording, the pause indicator flashes, the time display disappears, the COPY PROH indicator flashes and the recording operation will wait in a temporary pause mode. Once permission for recording is received, the COPY PROH indicator goes out and recording starts again.

It takes about 2 seconds for the unit to detect if recording is prohibited. It will look like the recording start/stop is delayed, however the record start/stop is being control in the correct changeover position using the digital delay memory function.

• SCMS Monitor Function

It is possible to monitor whether or not recording is possible in the recording standby state or in DA converter mode.

• COPY PROH indicator is lit : Recording is not possible.
• COPY PROH indicator is off : Recording is possible.

Cautions Before Recording

When the source equipment is CD, DAT, MD or DCC, the enabled/prohibit of the digital recording is unspecified until the start of the music. If the music source is started after this unit starts recording and the played song is found to be record-protected, this unit stops recording and may create unnecessary tracks. Recording must be started after confirming the enabled/prohibit state with the SCMS monitor function.

7. IC INFORMATION

- The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

■ PD4468D (IC701)
Mode control microcomputer

• Outline of Function

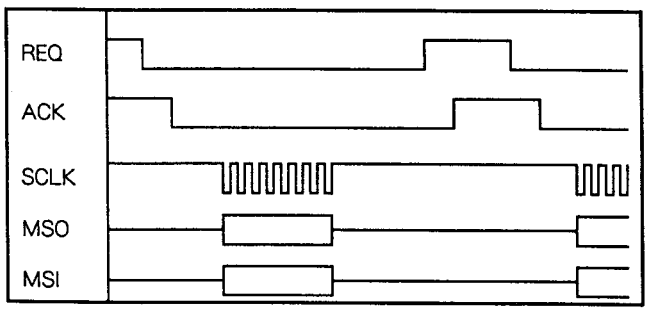
1. Function key input analysis
   Key matrix system by 8 outputs × 4 inputs (32 keys).
2. Remote control input analysis
   Double code which is conformed to standard.
3. FL display output
   Dynamic scan system.
   Improve the sound quality by display OFF.
   Control of LED driver IC.
4. Level detection and level meter display
   Communicate with level meter IC.
   Display the level meter.
   Display the peak margin.
5. Communicate with the mechanism control
   Read/transfer the mechanism operation, disc, disc inner time and skip informations.
6. Communicate with the C/U decode microcomputer
   Read the C bit, U bit and UNLOCK informations.
   Transfer the system control command.
   Realization of auto track number and auto record pause functions.
7. Digital attenuator IC control
   Realization of the fade function (Record/Playback).
8. Mechanism control function
   Record/Playback, Tuning operation, program playback, fade and skip etc.
9. Conform to SCMS (Serial Copy Management System).

• Pin Functions

No.	Port Name	Name	I/O	Active	Function	No.	Port Name	Name	I/O	Active	Function
1	RESET	—	IN	—	Reset input (L : Reset)	26	Vdd	+5V	—	—	+5V power supply voltage
2	T0	GRID 0	OUT	L	Grid outputs for FL display. (Dynamic scan system)	27	S3	SEGMENT 3	OUT	L	Segment outputs for FL display. (Dynamic scan system)
3	T1	GRID 1				28	S2	SEGMENT 2			
4	T2	GRID 2				29	S1	SEGMENT 1			
5	T3	GRID 3				30	S0	SEGMENT 0			
6	T4	GRID 4				31	P00	MREQ	IN	—	Serial bus communication required signal input. (Note 1)
7	T5	GRID 5				32	SCK	FSCK	I/O	—	Serial bus clock input / output. (Note 1)
8	T6	GRID 6				33	S0	FS0	OUT	—	Serial bus data output. (Note 1)
9	T7	GRID 7				34	SI	FSI	IN	—	Serial bus data input. (Note 1)
10	T8	GRID 8				35	P10	REMOTE	IN	—	Remote control signal input. Input the signal which eliminating the carrier element by remote sensor.
11	T9	GRID 9				36	P11	WORK	IN	—	C / U decode microcomputer communication control. (Note 5)
12	S15	SEGMENT 15	OUT	L	Segment outputs for FL display. (Dynamic scan system)	37	P12	UNLOCK	IN	—	Digital interface lock detection.
13	S14	SEGMENT 14				38	P13	———	IN	—	Not used.
14	S13	SEGMENT 13				39	P20	XRD	OUT	H	PD2020 control signal output. (Note 2)
15	S12	SEGMENT 12				40	P21	CUREQ	OUT	H	C/Udecode microcomputer communication control. (Note 5)
16	S11	SEGMENT 11				41	P22	XRESET	OUT	L	Main reset signal output.
17	S10	SEGMENT 10				42	P23	MACK	OUT	H	Serial bus handshake signal output. (Note 1)
18	Vload	− 30V	—	—							
19	Vpre	− 4V	—	—							
20	S9	SEGMENT 9	OUT	L	Segment outputs for FL display. (Dynamic scan system)						
21	S8	SEGMENT 8									
22	S7	SEGMENT 7									
23	S6	SEGMENT 6									
24	S5	SEGMENT 5									
25	S4	SEGMENT 4									

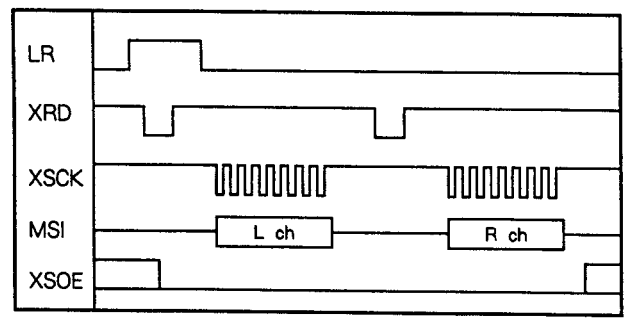
No.	Port Name	Name	I/O	Active	Function
43	P30	CUACK	OUT	H	C/U decode microcomputer communication control. (Note 5)
44	P31	CDR/CD	IN	—	Remote control switching input. Input pin for switch the remote control mode (CD/CD-R). Switch by the MODE switch at rear of the main unit.(H: CD, L: CD-R)
45	P32	OPT2/OPT3	IN	—	OPT2 and OPT3 switching input (H : OPT2 , L : OPT3)
46	P33	SKIP OFF	IN	—	Skip ON/OFF switching input. Input pin for switch the skip mode.
47	P60	KS0/LR	OUT	H	Key matrix outputs/PD2020 communication controls. (Note 2)
48	P61	KS1/XSOE			
49	P62	KS2/ALAT	OUT	H	Key matrix output/PD0026A communication control. (Note 3)
50	P63	KS3/DLAT	OUT	—	Key matrix output / MB88306P communication control. (Note 4)
51	P40	KSEL 4	OUT	—	Key matrix outputs.
52	P41	KSEL 5	OUT	L	
53	P42	KSEL 6			
54	P43	KSEL 7			
55	PP0	PREQ	OUT	H	Preliminary output. Not used.
56	X1	—	—	—	Connect the ceramic resonator.
57	X2	—	—	—	
58	Vss	GND	—	—	GND
59	XTI	GND	—	—	GND
60	XT2	—	—	—	Not used.
61	P50	DATA 0	IN	—	Key matrix inputs for function inputs.
62	P51	DATA 1			
63	P52	DATA 2			
64	P53	DATA 3			

(Note 1)
Mechanism control microcomputer (hereafter referred to as the mechanism controller) communication pins (pins 31 to 34 and 42). Perform serial communication with the mechanism controller.
Communicates 12 bytes of data each time.



Communication is performed as follows.
① The mechanism controller sets the REQ (communication request) signal to L.
② This microcomputer sets the ACK (communication authorization) signal to L.
③ The mechanism controller serially transfers 1 byte of data and then sets the REQ signal to H.
④ This microcomputer sets the ACK signal to H when the serial transfer is successfully completed.
⑤ Steps ① through ④ are repeated until the transfer of 12 bytes of data is completed.
* The mechanism controller and this microcomputer observe the state of the control line from each other, and communication processing signals will be interrupted if the transfer conditions do not materialize within a certain time.

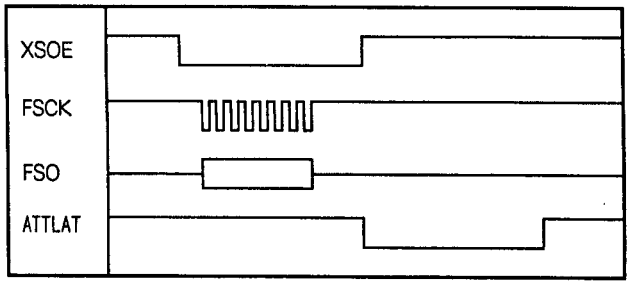
(Note 2)
Digital level meter communication pins (pins 39, 47 and 48). This microcomputer communicates with the digital level meter IC during a pause in communication with the mechanism controller, indicates the level on the FL display, and creates music-interval signals.



The communication format is as follows.
The channel for data readout is selected with LR signals. Select Lch with "H" and Rch with "L".
By setting the XRD signal to "L", the peak hold data is sent to the shift register for serial output of the microprocessor interface and the peak hold register is cleared at the same time.
Serial data is output with LSB first 8 bits. MSB serves as the overflow flag.
The data format obtainable through communication is shown below.

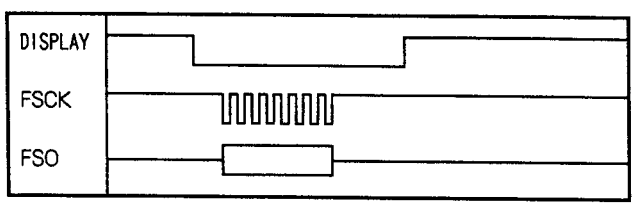
bit	7	6~0
	Overflow	90~24dB (1dB step)

(Note 3)
Digital attentuator IC (PD0026A) communication pin (pin 49).
Common with the key matrix output port and realizes the functions through key detection.
Communication transmits 1 byte of data one-way only from this microcomputer to the digital attentuator.
The communication format is as follows.



Communication is performed as follows.
① When this microcomputer detects a key input, it serially transfers the attentuator data when XSOE is L.
② When this microcomputer detects a key input, the data transferred in step ① above is latched when ATTLAT is L.
③ The data acquirable through communication are 177 steps of MAX 10110000 (ATT: 0 dB) to MIN 00000000 (ATT : -∞) with MSB first 1 byte binary.

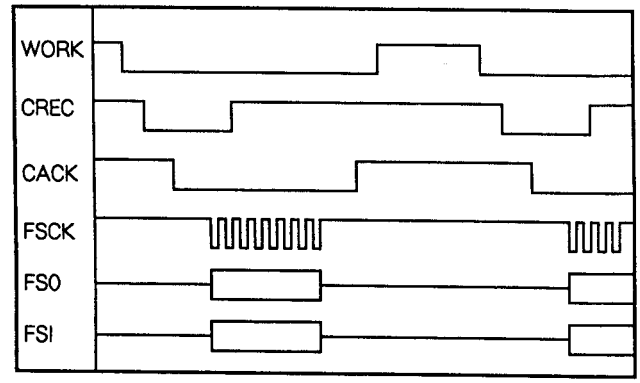
(Note 4)
LED driver IC (MB88306P) communication pin (pin 50).
Common with the key matrix output port and realizes the functions through key detection.
Communication transmits of MSB first 1 byte data one-way only from this microcomputer to the LED driver.
The communication format is as follows.



Communication is performed as follows.
① When this microcomputer detects a key input, it serially transmits the driver data when DISPLAY is L. The data is latched from the shift register.
② The communication data is configured as follows.

bit	7	6	5	4	3	2~0
	OPT1	OPT2	COAX	ANALOG	DISPOFF	REC LED

(Note 5)
C/U decoder microcomputer communication pins (pins 36, 40, and 43). This microcomputer communicates with the C/U decoder microcomputer.
The communication format is shown below.



Communication is performed as follows.
① Waits until the C/U decoder microcomputer finishes creating transmission data (WORK is L). (BUSY)
② This microcomputer sets the CREQ (communication request) signal to L.
③ The C/U decoder microcomputer sets the CACK (communication authorization) signal to L.
④ This microcomputer serially transfers 1 byte of serial data and sets the CREQ signal to H at the same time.
⑤ The C/U decoder microcomputer sets the CACK signal to H when the serial transfer is successfully completed.
⑥ Steps ② through ⑤ are repeated until the transfer of 12 bytes of data is completed.

* The C/U decoder and mode-control microcomputers interrupt communication processing if the transfer conditions do not materialize within a certain time.

■ GGC1056 (IC228)
(UPD78323GJ - 5BJ)
Mechanism Control Microcomputer

1. Pin Functions

No.	Mark	Name	I/O	Active	Function
1	P43/AD3	AD3	I/O		Data address lines
2	P44/AD4	AD4			
3	P45/AD5	AD5			
4	P46/AD6	AD6			
5	P47/AD7	AD7			
6	P50/A8	A8	O	—	Address lines
7	P51/A9	A9			
8	P52/A10	A10			
9	P53/A11	A11			
10	P54/A12	A12			
11	P55/A13	A13			
12	NC	GND	—	—	Not used.
13	P56/A14	A14	O	—	Address lines
14	P57/A15	A15			
15	Vdd	+5V	—	—	Positive power supply voltage
16	AVss	GND	—	—	Ground for A/D converter
17	P70/AN0	XCUP	I	—	"L" at finish the clamp switch is upped.
18	P71/AN1	XCDW		—	"L" at finish the clamp switch is downed.
19	NC	GND	—	—	Not used.
20	P72/AN2	XLOP	I	—	"L" at finish the loading switch is opened.
21	P73/AN3	XLCL		—	"L" at finish the loading switch is closed.
22	P74/AN4	TEPP	I(A)	—	Tracking error peak to peak (for tracking gain adjustment).
23	P75/AN5	RFL		—	Upper side envelope of playback RF.
24	P76/AN6	RFB		—	Lower side envelope of playback RF.
25	P77/AN7	MACK	I	L	Serial handshake input "L" toward the mode controller.
26	AVref	+5V	I	—	Reference voltage input of A/D converter.
27	AVdd	+5V	—	—	Analog power supply of A/D converter.
28	Vdd	+5V	—	—	Positive power supply voltage.
29	P20/NMI	XPFAIL	I	L	"L"at detect the power outage.
30	P21/INTP0	FG		—	Spindle FG
31	P22/INTP1	SCOR		H	EFM decoder frame sync.
32	P23/INTP2	ATIP		L	ATIP by-phase signal.
33	P24/INTP3	ESYNC		H	EFM encoder frame sync.
34	P25/INTP4	XRFDT		L	"L" at detect the EFM playback RF signal.
35	P26/INTP5	TOCP		H	TOC position sensor.
36	P27/INTP6/TI	SENS		—	SENS signal for SONY servo IC.
37	NC	GND	—	—	Not used.
38	P30/TxD	XDECE	O	L	WPC ATIP decoder chip enable output . "L"
39	P31/RxD	XECE		L	Jig for the test. Enable output for reading. "L"
40	P32/SO/SBO	MSO		—	Serial transmission data output of clocked sync. system.
41	P33/SI/SBI	MSI	I	—	Serial transmission data input of clocked sync. system.

No.	Mark	Name	I/O	Active	Function
42	P34/SCK	MSCK	O	L	Serial transmission clock output of clocked sync. system.
43	NC	GND	—	—	Not used.
44	P80/T000	LTD	O	H	Serial and parallel port latch of LD power and loading system. "H"
45	P81/T001	LTS			Serial and parallel port latch of servo system. "H"
46	P82/T002	EFMCLV	O	—	Spindle servo EFM/$\overline{\text{Wobble CLV}}$ mode.
47	P83/T003	CLV	O	—	Spindle servo CLV/$\overline{\text{CAV}}$ mode.
48	P84/T010	SPSP		—	Spindle CAV target speed, lower 8 bit (PWMoutput).
49	P85/T011	MREQ		L	Serial handshake output toward mode control. "L"
50	RESET	XRST	I	L	Reset input. "L"
51	X2	CLOCK	I	—	Crystal connection pin for system clock oscillation. Connect to X1 pin when applying a external clock.
52	X1	CLOCK	—	—	
53	NC	GND	—	—	Not used.
54	Vss	GND	—	—	Ground.
55	WDTO	NC	O	—	Not used.
56	P00/RTP0	XSUBQE		L	EFM decoder. Subcode Q reading enable. "L"
57	NC	GND	—	—	Not used.
58	P01/RTP1	EENCE	O	H	EFM encoder. Serial enable. "H"
59	P02/RTP2	XASYNC		L	ATIP frame sync. "L"
60	P03/RTP3	XEXTSYN		L	EFM encoder. External sync. enable. "L"
61	P04/RTP4	SSQ	O	—	Serial data output for command of SONY servo IC .
62	P05/RTP5	SSCK	O	L	Serial clock output for command of SONY servo IC .
63	P06/RTP6	XLT			Command latch of SONY servo IC. "L"
64	P07/RTP7	RECE	O	H	Laser diode recording power ON. "H"
65	EA/Vpp	GND	I	—	External ROM mode by connecting to GND pin.
66	Vss	GND	—	—	Ground.
67	P93/TMD	RAME	O	H	Enable of SRAM. "H"
68	P92/TAS	XSVRST	O	L	Serial and parallel reset output of the servo system IC. "L"
69	P91/WR	XWR			Strobe signal output for read operation of external memory.
70	P90/RD	XRD			Strobe signal output for write operation of external memory.
71	ASTB	ASTB		H	Signal which is latched to the lower address signal for external memory access at external.
72	P40/AD0	AD0	I/O	—	Data address lines.
73	P41/AD1	AD1		—	
74	P42/AD2	AD2		—	

Note : I (A) Analog IN

2. Pin Functions of Periphery Mechanism Control ICs

• IC234 TC74HC574AP

No.	Mark	Name	I/O	Active	Function
12	Q7	DIRC	O	H	SONY servo IC DIRC "L"
13	Q6	(TP CRC)		—	Not used.
14	Q5	LDPW0		—	Lowermost bit output of recording laser power (D/A OUT).
15	Q4	(DMUTE)		—	Not used.
16	Q3	(TP 1P)		—	Not used.
17	Q2	(TNO C)		—	Not used.
18	Q1	(NAD L)		—	Not used.
19	Q0	SS P		L	Low speed port of line speed ("H" when line speed is within 1.3m/sec.).

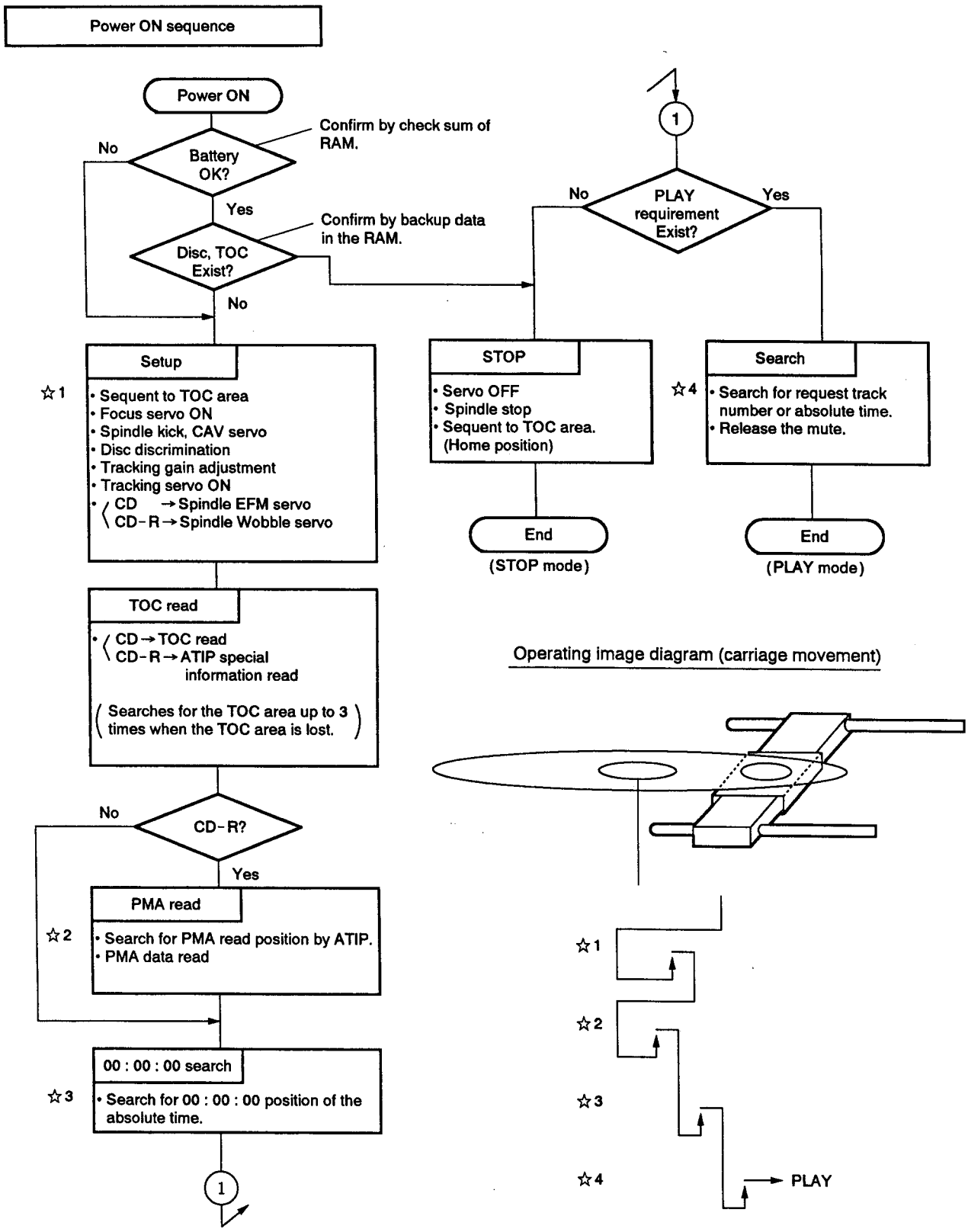
• IC205 TC74HC4094AP

No.	Mark	Name	I/O	Active	Function
4	Q0	TEG0	O	L	LSB ┐ Tracking error amp gain adjustment. MSB ┘
5	Q1	TEG1			
6	Q2	TEG2			
7	Q3	TEG3			Tracking error envelope detection reset . "L"
11	Q7	XAMUTE		L	Audio last step mute. "L" (conform to the mode controller.) Mute is ON when input selector is switched during REC PAUSE. Mute is ON during STOP.
12	Q6	XLDON		L	Laser diode OFF/$\overline{\text{ON}}$.
13	Q5	CDMIR		L	Selection SW of mirror detection circuit. CD/$\overline{\text{R CD}}$
14	Q4	—		L	Not used.

• IC232 TC74HC4094AP

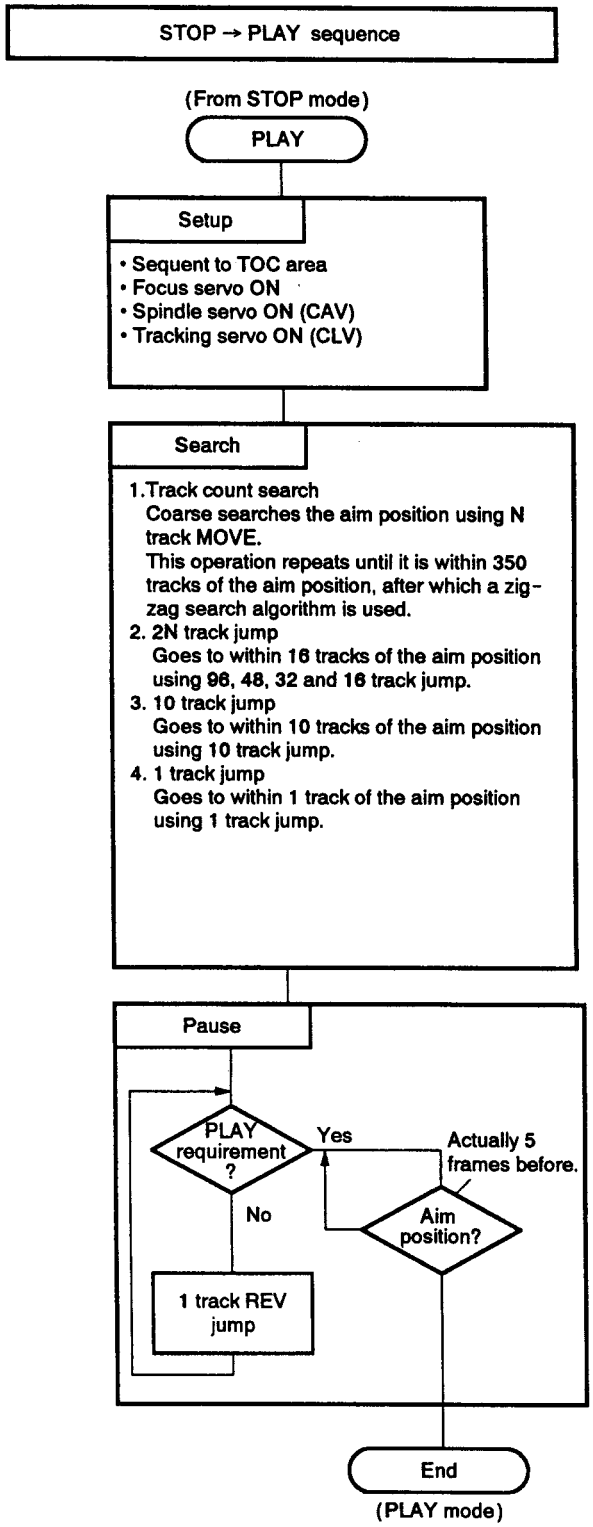
No.	Mark	Name	I/O	Active	Function
4	Q0	LDPW	O	L	LSB ┐ Lower 4 bit (D/A OUT) recording laser power setting. MSB ┘
5	Q1	—			
6	Q2	—			
7	Q3	—			
11	Q7	CUP		H	Clamper up.
12	Q6	CDWN			Clamper down.
13	Q5	LOUT			Loading open.
14	Q4	LIN			Loading close.

3. Operating Flow Chart (1)

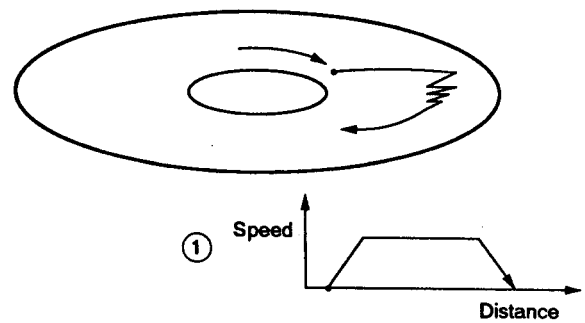


Note: For the operating flow chart of tracking gain adjustment, refer to pages 1-50 to 1-52.

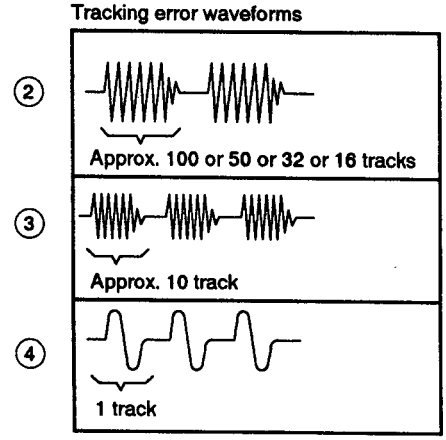
4. Operating Flow Chart (2)



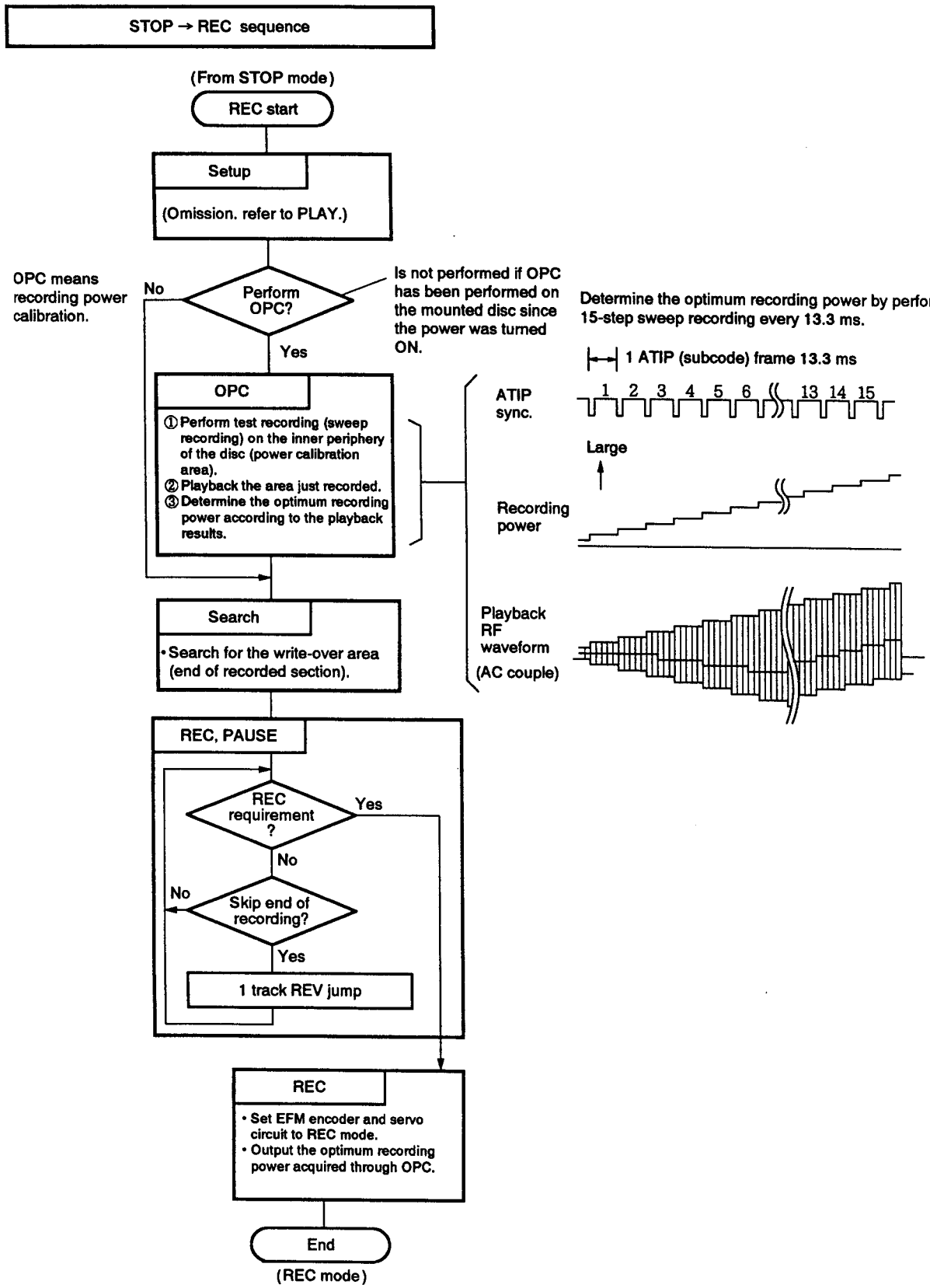
Operating image diagram



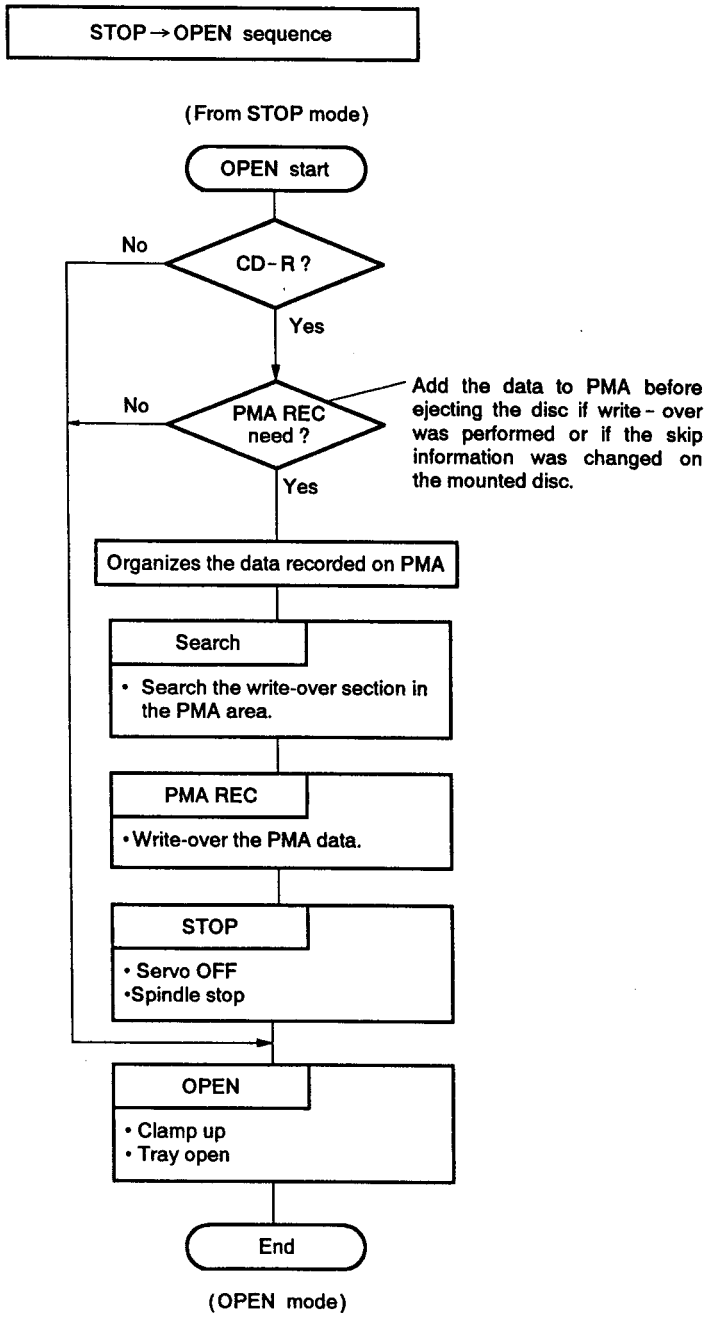
Tracking error waveforms



5. Operating Flow Chart (3)



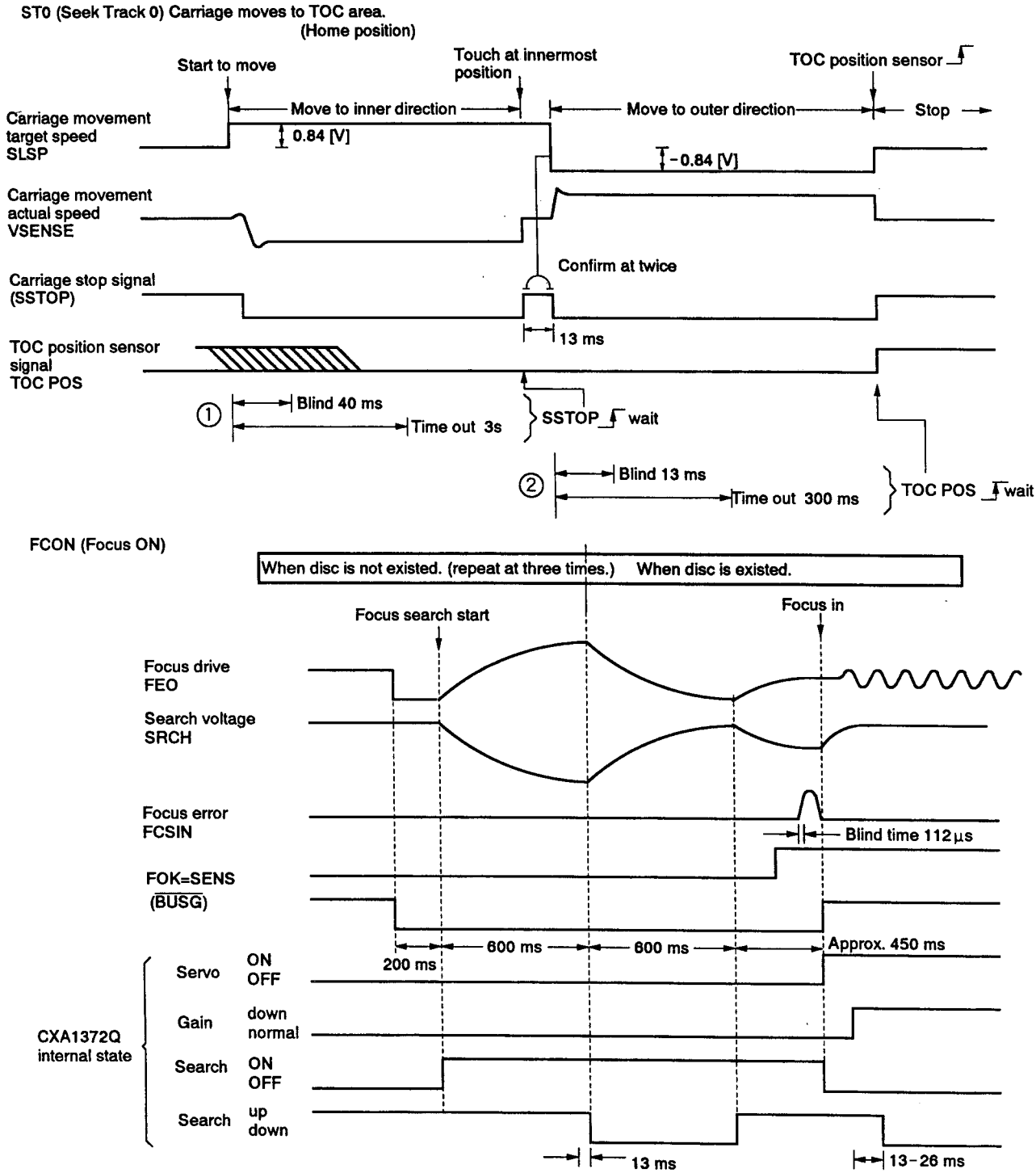
6. Operating Flow Chart (4)



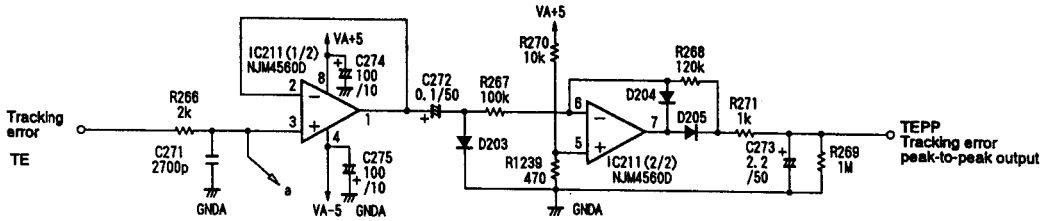
OPEN

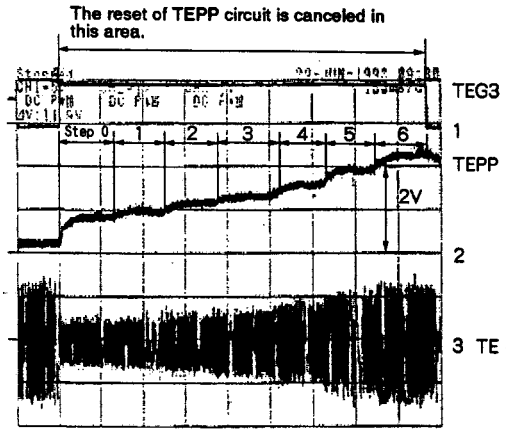
flashes on the display during these operations.

7. Timing Chart

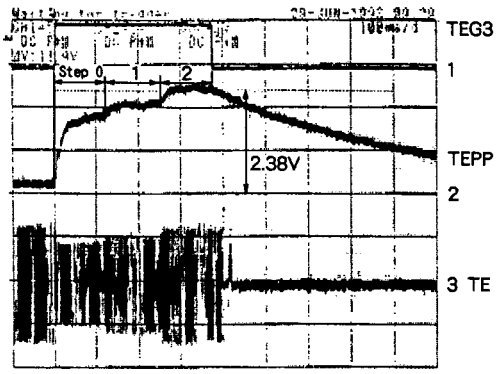


8. Tracking Error Signal Peak-to–Peak Detection Circuit



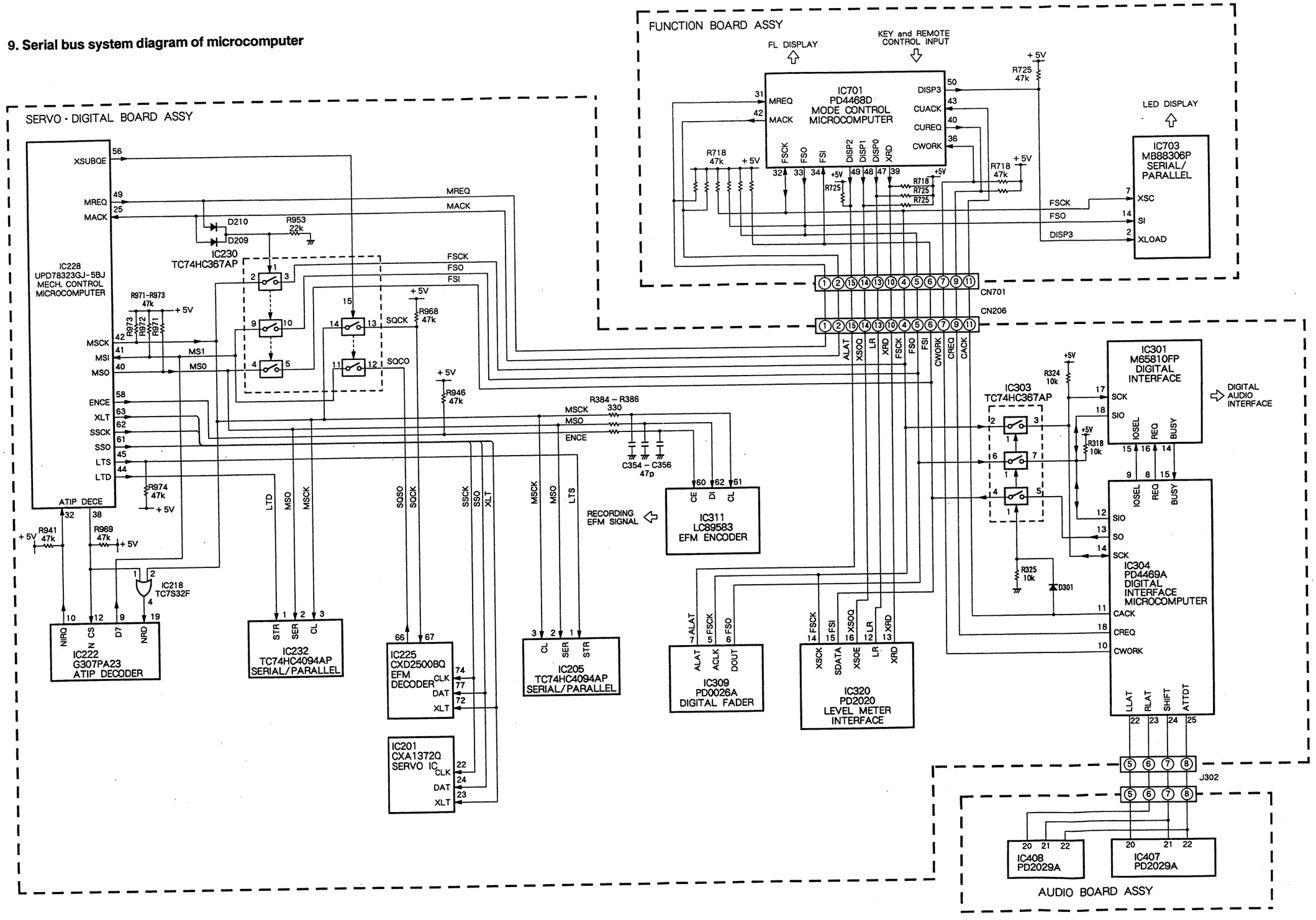


- With a CD
  The tracking error gain adjustment ends when the TEPP is greater than 2 V.



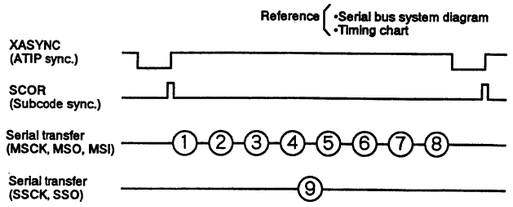
- With a CD-R
  The tracking error gain adjustment ends when the TEPP is greater than 2.38 V.

9. Serial bus system diagram of microcomputer



10. Outline of Serial Transfer Timing of the Mechanism Controller

The following serial transfer is performed with a standard cycle of 13.3 ms which has been synchronized to either ATIP sync signals (with CD - R) or playback subcode sync signals (with CD).
There are two serial bus systems.



① ATIP decoder communication format
Readout every 4 bytes (32-bit) of ATIP data from the G307PA23 ATIP decoder. The readout starts only when the ATIP decoder has decoded values (ATIP connector is L).

② Readout (reception) of playback subcode Q data
Readout the 10-byte subcode Q data of each subcode frame from the CXD2500BQ EFM decoder.
The readout is done only when CXD2500BQ has decoded values.

③ Expansion port output 1 in the Servo•digital board assy
Output 1 byte to IC205 (TC74HC4094AP) which has been latched to serial/parallel.

④ Transmitting and receiving data with the mode control CPU
Transmit and receive 12 bytes of data using a hand-shake line.

⑤ Mode setting output for the EFM encoder
Used to set the operation mode of the LC89583 EFM encoder. Transfer 8 bytes of data when the power is first turned on and 7 bytes thereafter.

⑥ Expansion port output 2 in the Servo•digital board assy
Output 1 byte of data to the IC232 (TC74HC4094AP) serial/parallel latch.

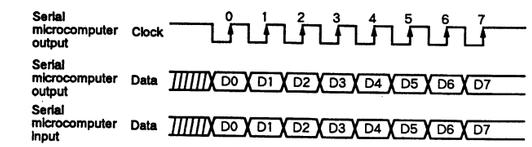
⑦ Output of recording subcode Q data
Sets the 10-byte subcode Q data and the 1-bit P data to be recorded in the next subcode frame for the LC89583 EFM encoder. Command transmissions of 1 byte accompany this setting both before and after for a total transfer of 12 bytes.

⑧ Test signal

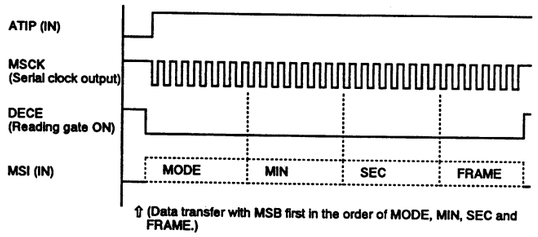
⑨ Servo system command setting output
Sets the operation mode for IC201 (CXA1372Q) and IC225 (CXD2500BQ). It occurs at the timing shown in the above figure, but serial transfer may occasionally occur to match the servo timing during search operation.

11. Serial Transfer Timings

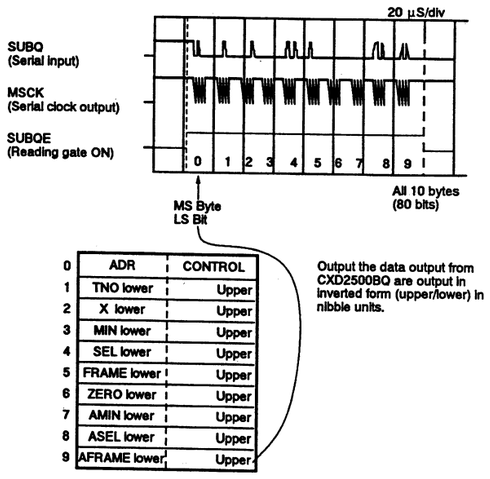
Standard timing (all 8 - bit units)



① ATIP data mechanism control serial input (MSCK serial clock : 1 MHz) (IC222 G307PA23)

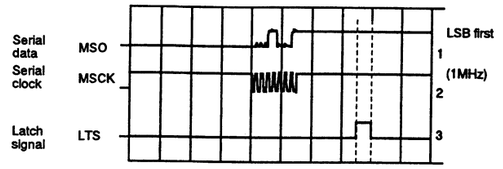


② Readout timing of playback subcode Q data (IC225 CXD2500BQ)



	ADR	CONTROL
0	TNO lower	Upper
1	X lower	Upper
2	MIN lower	Upper
3	SEL lower	Upper
4	FRAME lower	Upper
5	ZERO lower	Upper
6	AMIN lower	Upper
7	ASEL lower	Upper
8	AFRAME lower	Upper

③ Output timing of the serial expansion port on the servo board (IC205 TC74HC4094AP)

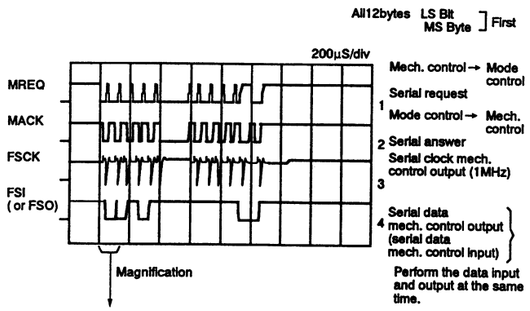


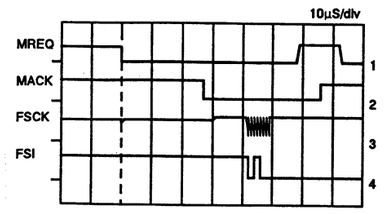
LSB first 8 bit

Bit	
0	TEG 0
1	TEG 1
2	TEG 2
3	SSEL
4	
5	CD MIR
6	XLDON
7	XAMUTE

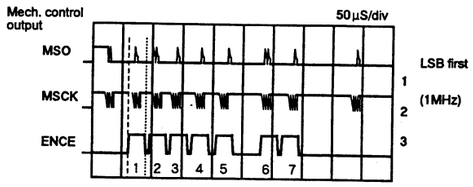
(Not used)

④ Serial data transfer to the mode-control CPU (IC701 PD4468D)



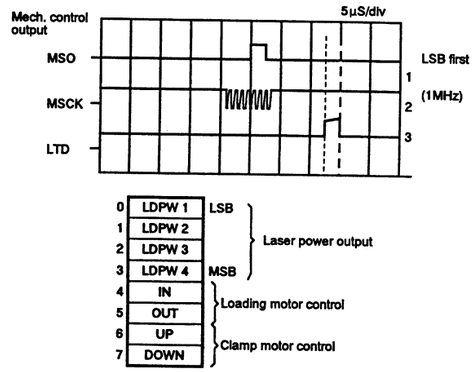


⑤ Mode (command) setting output timing to EFM encoder



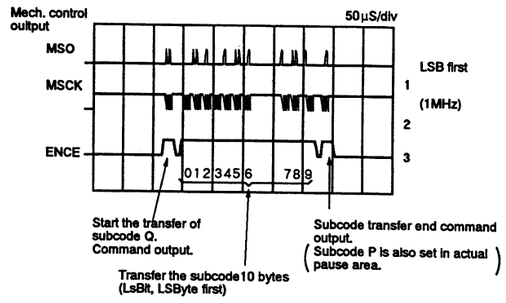
The EFM encoder commands consist of 8 different types (4-bit data each). Through serial transfer, the eight types of commands are set (refreshed) when the power is first turned ON, and the seven types during normal operation.

⑥ Output timing from the serial expansion port in Servo•digital board assy (IC232 TC74HC4094AP)



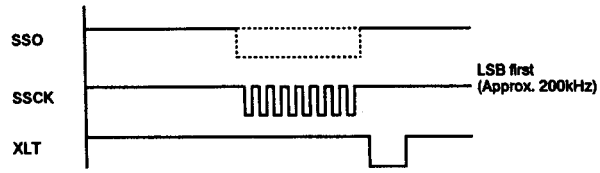
0	LDPW 1	LSB	Laser power output
1	LDPW 2		
2	LDPW 3		
3	LDPW 4	MSB	
4	IN		Loading motor control
5	OUT		
6	UP		Clamp motor control
7	DOWN		

⑦ Serial output of the recording subcode Q data to the EFM encoder (IC311 LC89583)

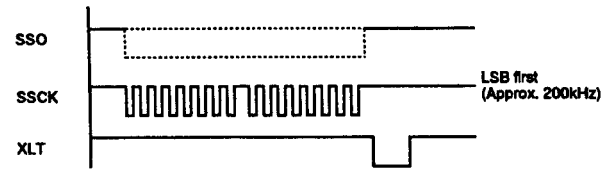


⑧ Servo system command setting serial output
(IC201 CXA1372Q, IC225 CXD2500BQ)

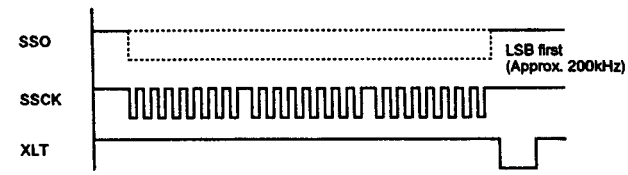
1) 8-bit command transfer



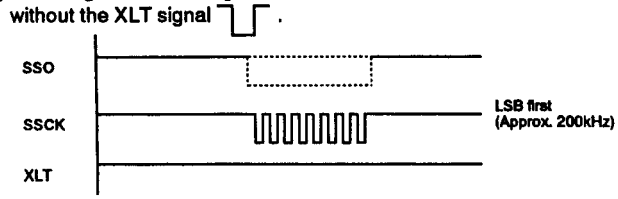
2) 16-bit command transfer



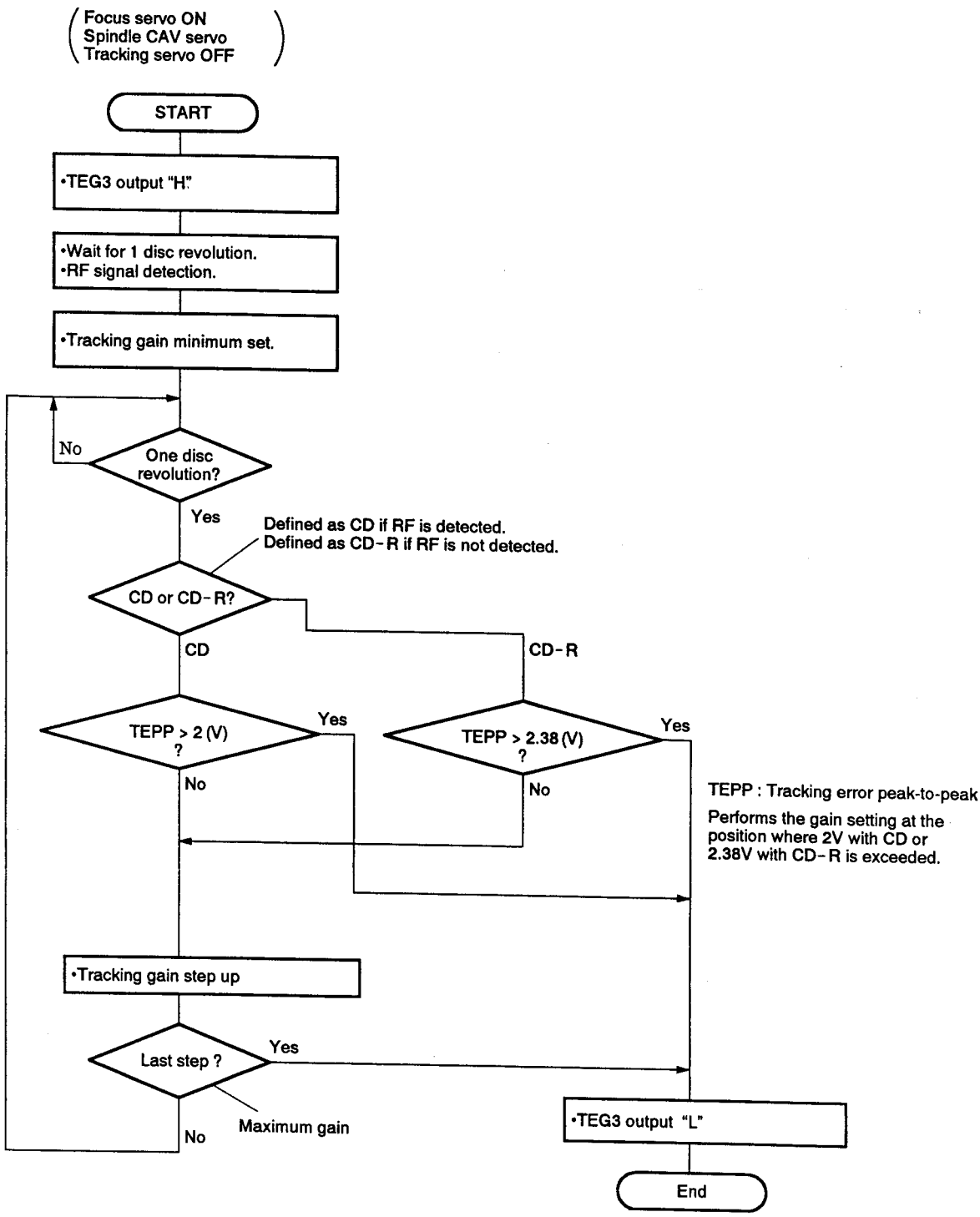
3) 24-bit command transfer



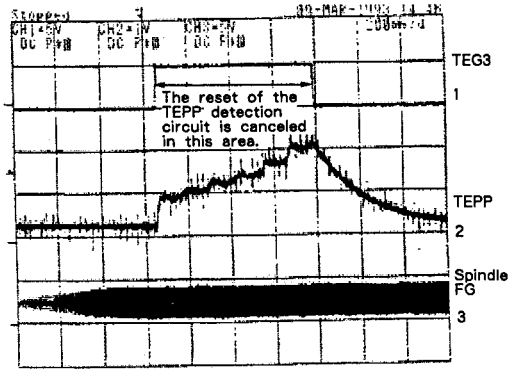
4) To change the SENS signal, the data transfer is also done without the XLT signal  .



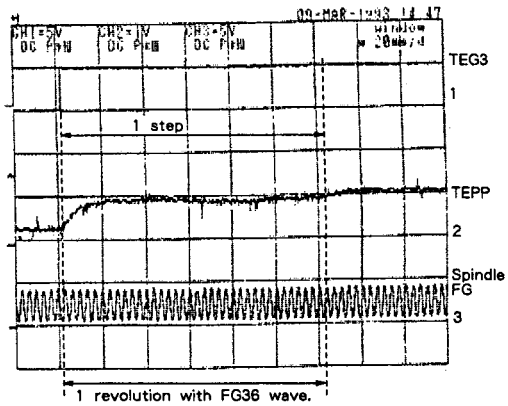
12. Tracking Gain Adjustment Operation Flow Chart



Status of tracking error peak-to-peak signal during tracking gain adjustment.



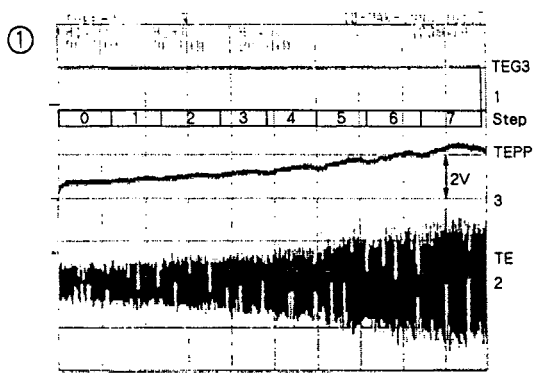
Enlarged diagram of 1 step.



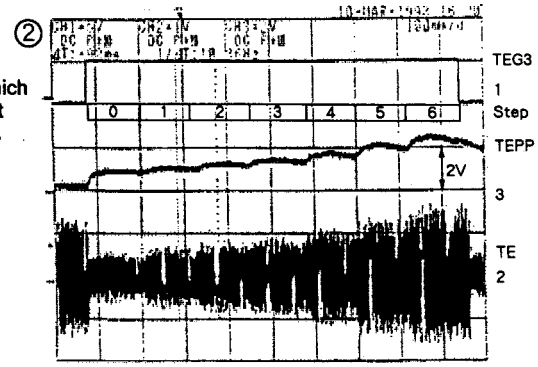
Timing chart of the tracking gain adjustment

The amplitude is set according to the steps where 2.0V TE peak-to-peak with CD or 2.38V TE peak-to-peak with CD - R is exceeded.

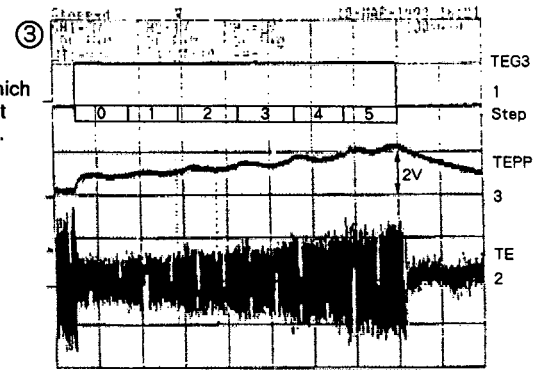
① Example in which the disc gain is small and raised to the maximum.
The specified gain is exceeded in step 7.



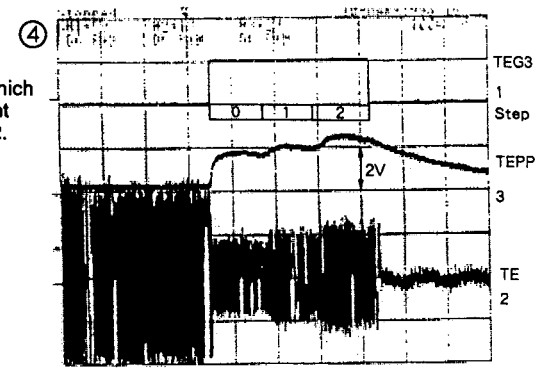
② Example in which the adjustment ends in step 6.



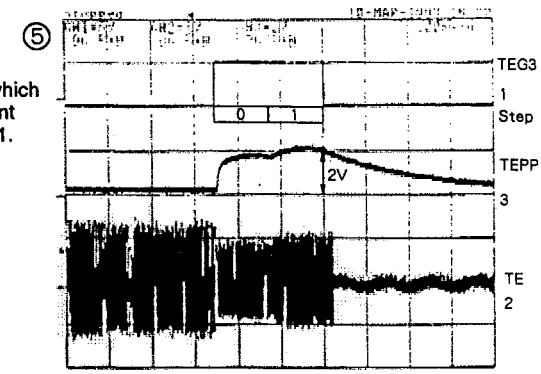
③ Example in which the adjustment ends in step 5.



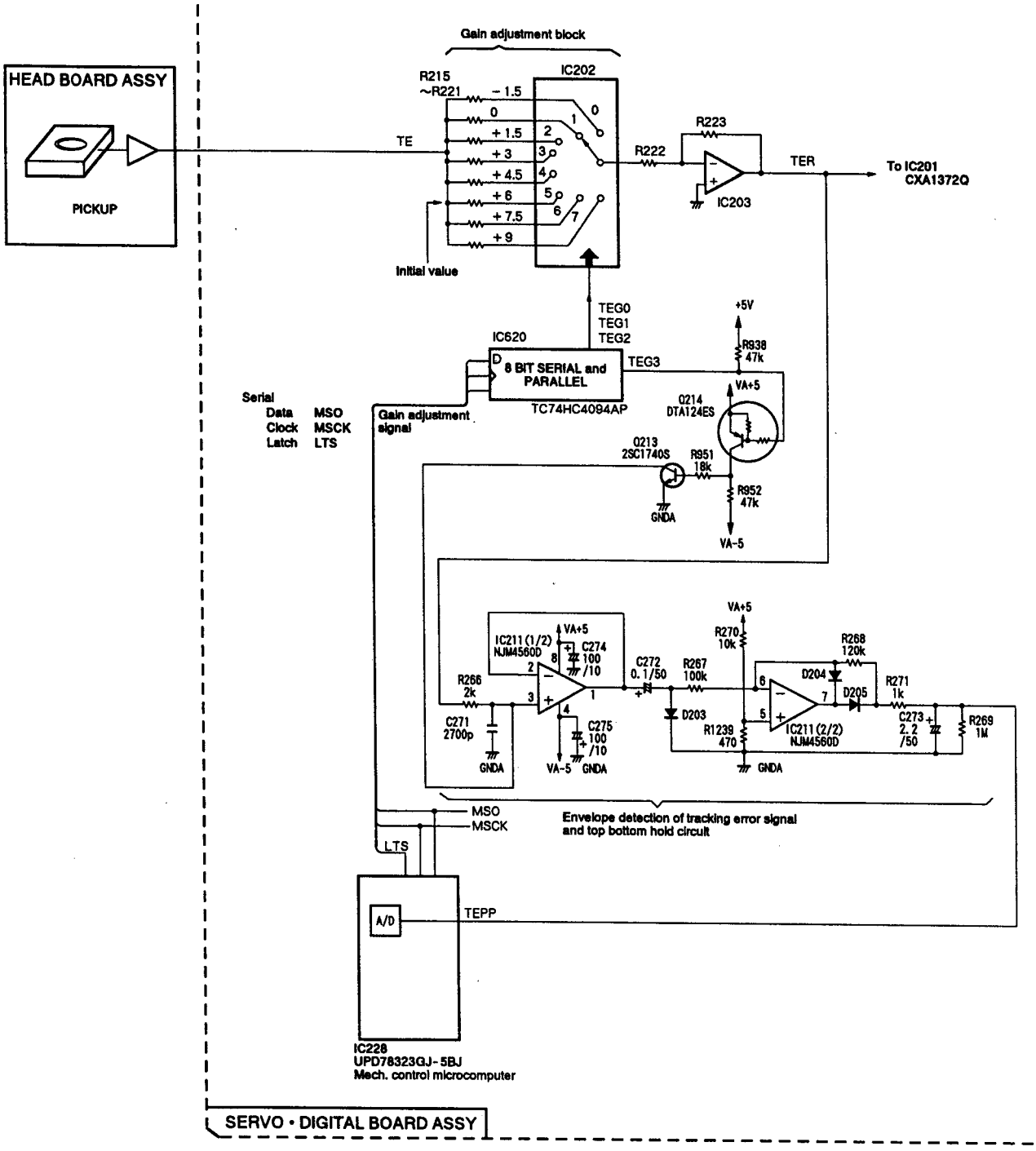
④ Example in which the adjustment ends in step 2.



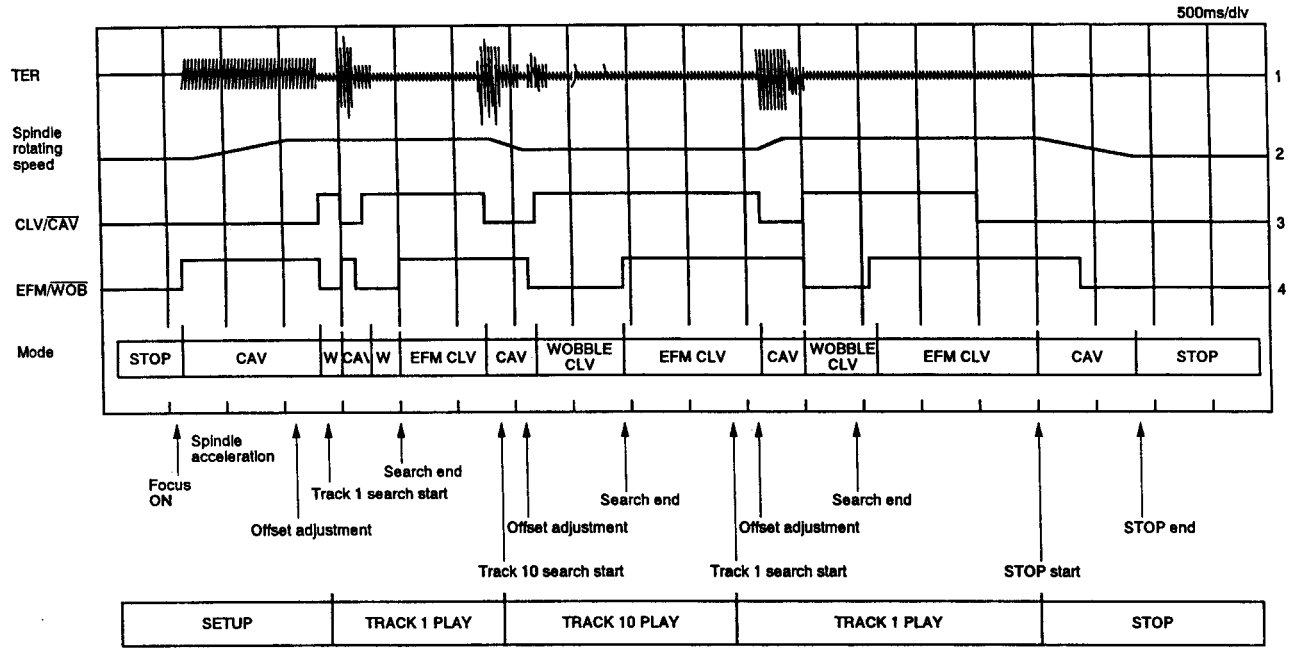
⑤ Example in which the adjustment ends in step 1.



13. Circuit Diagram of Tracking Gain Adjustment

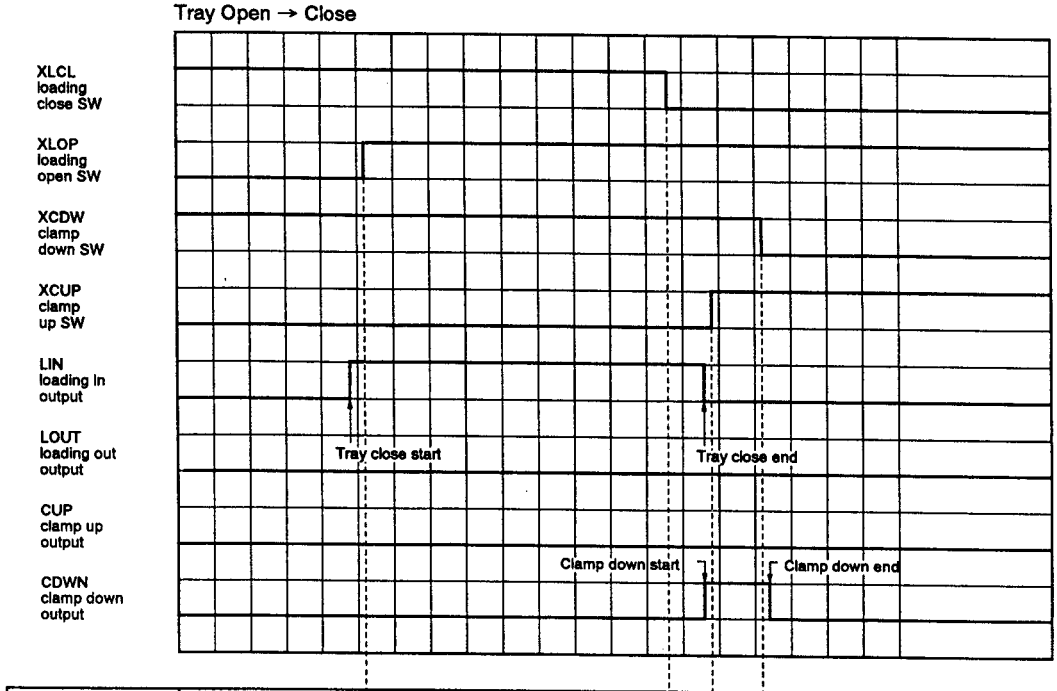


14. Spindle Servo Mode Switch in CD-R STOP → PLAY → SEARCH → STOP Operation



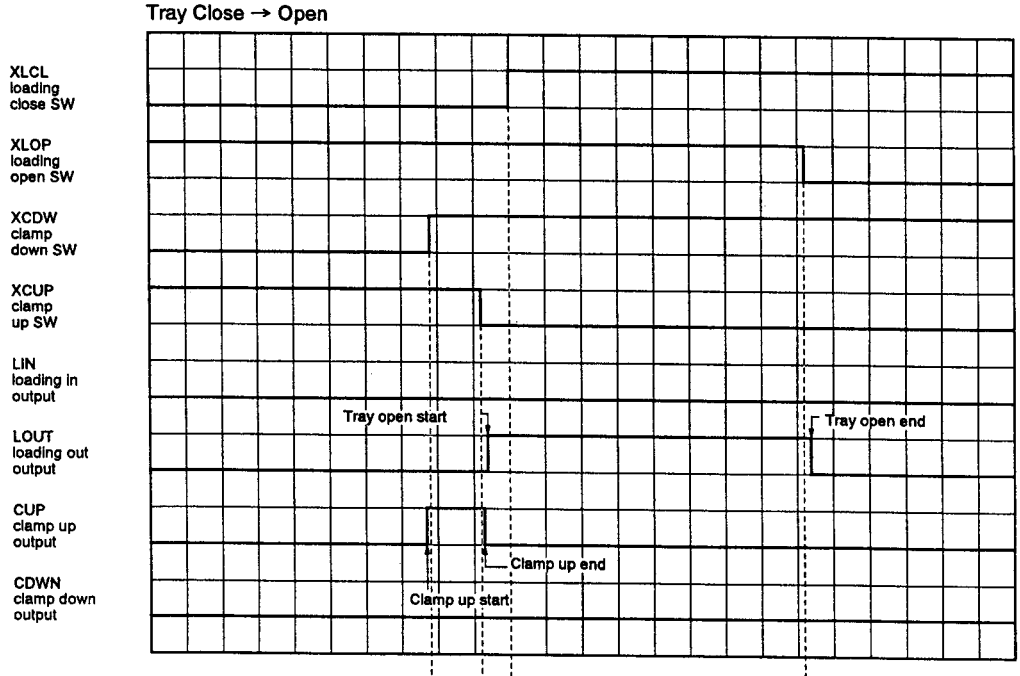
15. Open • Close Operation Timing Chart

Tray Open → Close



Loading state	Open end	During close	Close end
Clamp state	Up end	During down	Down end

Tray Close → Open



Loading state	Close end	During open	Open end
Clamp state	Down end	During up	Up end

- Clamp standby state

The slider is locked so that it cannot move during shipping. When a disc is not mounted, the tray is set to this position.

Points: ① It is possible to move the slider only when the tray is in the clamped state. To open the tray, first move the slider to the TOC position.

② When the tray is in the clamped state, set the clamp down before performing the setup.

■ PD4469A (IC304)
C/U Decode Microcomputer

• Outline of Function

1. Digital interface IC control
   Digital input select
   C-bit reading
   UNLOCK detection
2. Periphery digital circuit control
   Crystal ON/OFF
   Clock select
   FS converter control
   VCO ON/OFF
3. Control and communication of memory control IC (PD6107A)
   U bit reading
   Memory circuit control
4. Audio circuit control
   DAC control
   Emphasis control
5. Communicate with mode control.
   Transfer the C-bit, U-bit and UNLOCK informations.
   Command reception from mode control.

• Pin Functions

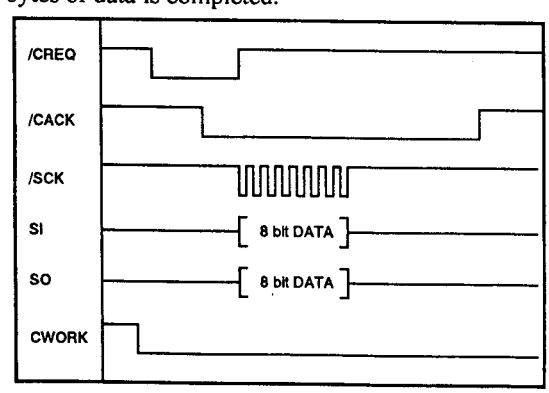
No.	Mark	Name	I/O	Function	No.	Mark	Name	I/O	Function
1	XT1	——	—	Ground.	22	P23	LLAT	O	DAC control LATCH Lch
2	XT2	——	—	Not used.	23	P22	RLAT	O	DAC control LATCH Rch
3	RSET	XRESET	—	CPU reset. ("L" : Reset)	24	P21	SHFT	O	DAC control SHIFT
4	X1	——	—	Main system clock oscillation. (4.194304MHz)	25	P20	ATTDT	O	DAC control serial data
5	X2	——			26	P73	XEMP	O	Deemphasis control output. ("H": OFF, "L": ON)
6	P33	FSC	O	FS conversion permit signal. ("H" : FS conversion)	27	P72	XOPT	O	OPT input permit. ("L": permit, "H": forbid)
7	P32	XFEN	O	VCO oscillation control. (L = permit)	28	P71	ECSEL	O	EFM encoder clock selection. ("H": Xtal, "L": VCO)
8	P31	REQ	O	M65810FP communication request signal. ("H": I/O enable)	29	P70	ACSEL	O	DA converter clock selection. ("H": Xtal, "L": VCO)
9	P30	IOSEL	O	M65810FP input and output switch. ("H" : MICON→LSI)	30	P63	XXTL	O	Xtal osc. control output. ("H": OFF, "L": ON)
10	P81	CWORK	O	Mode control communication. ("H":forbid, "L":permit)	31	P62	FS32	O	fs=32kHz selection output. (H : fs=32kHz)
11	P80	CACK	O	Mode control communication acknowledge.	32	P61	MLAT	O	Playback mode selection output. PD6107A command register latch pulse. (L : PB)
12	SI	SIO	I/O	Serial input and output data.					
13	SO	SO	O	Serial output.	33	P60	XUSEL	O	U-bit data selection. (L : U-bit READ, H : OUTPUT)
14	SCK	SCK	I/O	Serial clock.	34	P53	QH	I/O	U-bit data/control data.
15	P00	BUSY	I	M65810FP BUSY output.	35	P52	QG		
16	P13	VCUL	I	VCO unlock. ("H" : UNLOCK, "L" : LOCK)	36	P51	QF		
17	INT2	ULAT	I	Reading end interruption of U code 1 byte .	37	P50	QE		
18	INT1	CREQ	I	Communication request interruption from main microcomputer.	38	P43	QD		
					39	P42	QC		
19	INT0	UNLOCK	I	M65810FP unlock signal.	40	P41	QB		
20	NC	——	—	Not used.	41	P40	QA		
21	VDD	VDD	—	5V	42	VSS	GND	—	Ground.

• Description of functions and operation format

• Communication with mode controller
Communication conditions
CWORK is H when creating C-bit and U-bit data, and L at all other times. The L section is 13.3 mS to 62.4 mS. In this section, serial communication is performed if there is a /CREQ signal from the mode controller. Request signals are not accepted in the H section.

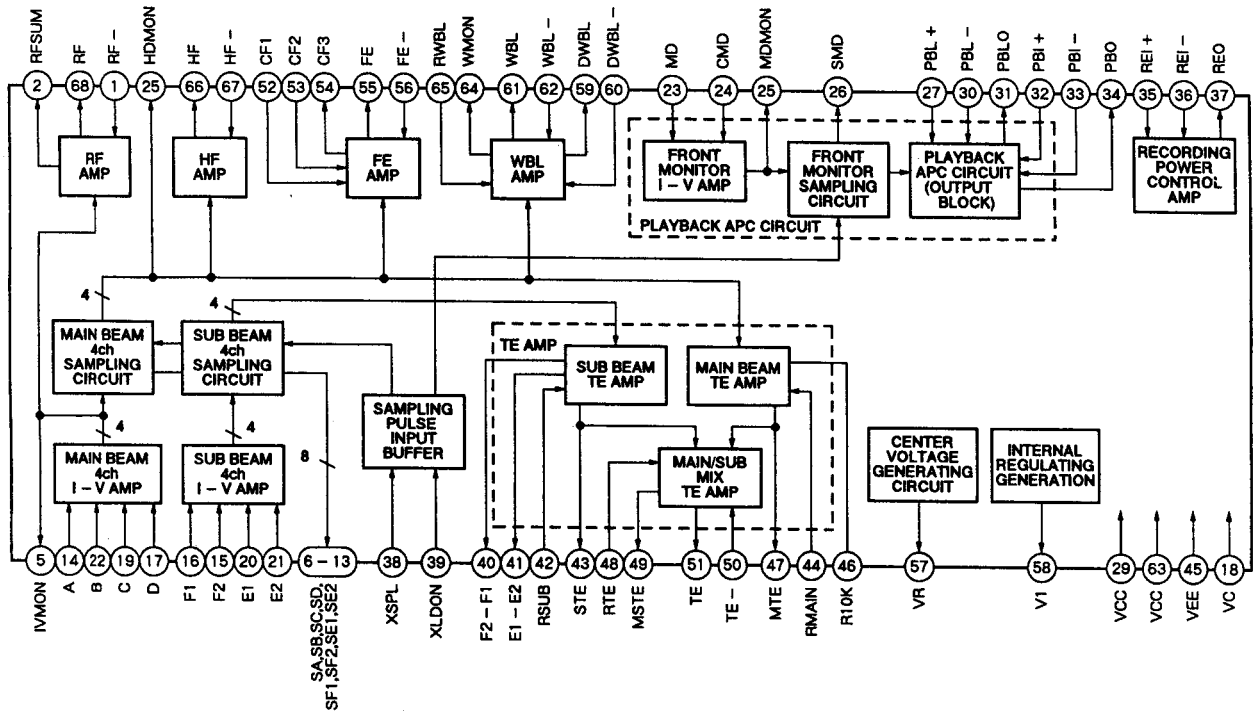
• CREQ, CACK, SI, SO, SCK and CWORK
This microcomputer performs handshake with the mode controller as follows.

1. The mode controller sets the /CREQ signal to L.
2. This microcomputer sets the CACK (communication approval) signal to L.
3. After the mode controller sets the /CREQ signal to H, 1 byte of serial data is transferred. (512 kHz transfer clock)
4. This microcomputer sets the CACK signal to H when communication succeeds.
5. Steps 1 through 4 are repeated until the transfer of 12 bytes of data is completed.



■ PA4020A (IC101)
RF Amplifier IC

• Block Diagram



• Pin Functions

No.	Name	I/O	Function	No.	Name	I/O	Function
1	RF –	I	RF amp – (minus) input.	21	E2	I	Detector inputs.
2	RFSUM	O	RF summing amp output.	22	B		
3	HDMON	O	Sample hold signal monitor.	23	MD	I	Monitor diode input.
4	VEE	—	Power supply voltage. (– 5V)	24	CMD	I	I-V conversion OP amp + input for playback laser APC.
5	IVMON	O	I-V amp output monitor.	25	MDMON	O	I-V conversion OP amp output for playback laser APC. (Monitor terminal)
6	SA	O	Connect capacitors for sample hold.	26	SMD	O	Hold output for playback laser APC.
7	SB			27	PBL+	I	Loop gain setting OP amp + input for playback laser APC.
8	SC			28	NC	—	NC
9	SD			29	VCC	—	Power supply voltage. (+5V)
10	SF1			30	PBL –	I	Loop gain setting OP amp – input for playback laser APC.
11	SF2			31	PBLO	O	Loop gain setting OP amp output for playback laser APC.
12	SE1			32	PBI+	I	OP amp + input for converting voltage and current of playback laser APC.
13	SE2			33	PBI –	I	OP amp – input for converting voltage and current of playback laser APC.
14	A	I	Detector inputs.	34	PBO	O	OP amp output for converting voltage and current of playback laser APC.
15	F2						
16	F1						
17	D						
18	VC	I	Center voltage. (GND)				
19	C	I	Detector inputs.				
20	E1						

No.	Name	I/O	Function	No.	Name	I/O	Function
35	REI+	I	OP amp + input for setting the current of recording laser power .	49	MSTE	O	DPP signal output.
				50	TE −	I	OP amp − input for TE level adjustment.
36	REI −	I	OP amp − input for setting the current of recording laser power .	51	TE	O	OP amp output for TE level adjustment.
				52	CF1	I	Connect capacitors for FE bandpass limited.
37	REO	O	OP amp output for setting the current of recording laser power .	53	CF2	I	
				54	CF3	O	
38	XSPL	I	Sample pulse input. L (0V) : Sample, H (5V) : Hold	55	FE	O	OP amp output for FE level adjustment.
				56	FE −	I	OP amp − input for FE level adjustment.
39	XLDON	I	ON/OFF input of laser diode. L (0V) : ON, H (5V) : OF F	57	VR	O	Center voltage generating circuit output.
				58	V1	O	Internal power supply voltage monitor.
40	F2 − F1	O	Sub beam PP monitor output.	59	DWBL	O	OP amp output for LPF of wobble balance circuit.
41	E1 − E2	O	Sub beam PP monitor output.	60	DWBL −	I	OP amp − input for LPF of wobble balance circuit.
42	RSUB	I	Volume pin for sub beam gain difference adjustment.	61	WBL	O	Wobble signal output.
43	STE	O	Sub beam gain differntial monitor output.	62	WBL −	I	OP amp − input for generating wobble signal.
44	RMAIN	I	Volume pin for main beam tracking balance adjustment.	63	VCC	—	Power supply voltage .(+5V)
				64	WMON	O	PP signal monitor for wobble.
45	VEE	—	Power supply voltage. (− 5V)	65	RWBL	I	Connect VCR of wobble balance circuit.
46	R10K	—	Internal resistor 10k Ω (for differntial amp of main beam : connect to RMAIN)	66	HF	O	HF signal output.
47	MTE	O	Differntial monitor of main beam.	67	HF −	I	HF amp − input.
48	RTE	O	Volume pin for main-sub gain differnce adjustment.	68	RF	O	RF signal output.

■ G307PA23 (IC222)
WPC (Wobble Processor)

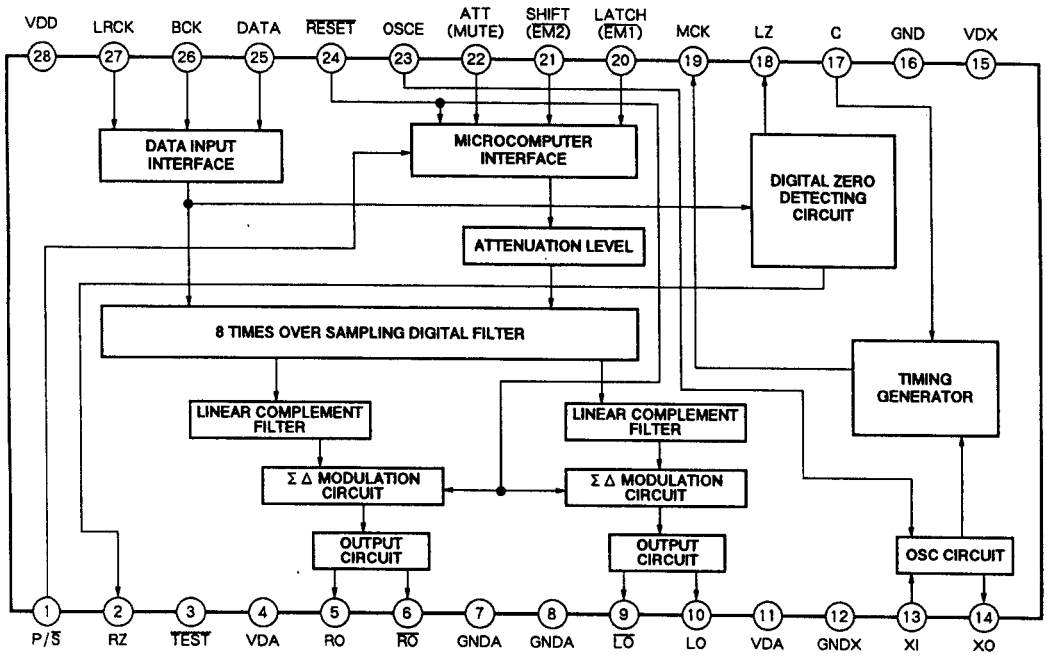
• Pin Functions

No.	Name	I/O	Function	No.	Name	I/O	Function
1	D0	ON4T	Data bus bit 0	20	SUBCSYNC	ICN	Subcode synchronous for ATIP sub code phase.
2	D1	ON4T	Data bus bit 1				
3	D2	ON4T	Data bus bit 2	21	WOBBLE	ISN	Digital wobble input. (a part of push-pull signal)
4	D3	ON4T	Data bus bit 3	22	CLK	ISNH	System clock input. (4.3218MHz) When normal CD speed (N=1), CLK is 4.3218MHz which is the same as the channel bit frequency of writing EFM signal.
5	D4	ON4T	Data bus bit 4				
6	VSS	—	Ground				
7	D5	ON4T	Data bus bit 5	23	VSS	—	Ground.
8	D6	ON4T	Data bus bit 6	24	MCSEL	ICN	Motor control selection (Input). When MCSEL = 0, internal motor control is ERRPWM. When MCSEL = 1, external (MSC pin 25) is ERRPWM.
9	D7	ON4T	Data bus bit 7 or serial output.				
10	NIRQ	ON40D	Interrupt request output. (Active : L)				
11	VCC	—	Power supply voltage. (5V ± 10%)				
12	NCS	ICN	Output enable for D0 − D7. (Active : L)	25	MSC	ISN	External motor speed control (Input).
13 | 17	NC	—	Not used.	26	ERRPWM	ON40D	Motor control output (open-dorein).
18	SEPPAR	ICN	μ C interface selection. When SEPPAR=0, select parallel μ C interface. When SEPPAR=1, select serial μ C interface.	27	SCN	ICN	Scan pass enable (Active : L). Scan pass is used only while this IC is produced. Generally, SCN is active High.
19	NRD	ICN	Reading control input. (Active : L)	28	VCC	—	Power supply voltage. (5V ± 10%)

Note; ISNH =CMOS non-inverting schmitt trigger input clock driver.
ISN =CMOS non-inverting schmitt trigger input.
ON40D =Open-dorein output 4mA (current decrease).
ON4T =3 states output 4mA (current decrease).

■ PD2029A (IC407, IC408)
DA Converter IC

• Block Diagram



• Pin Functions

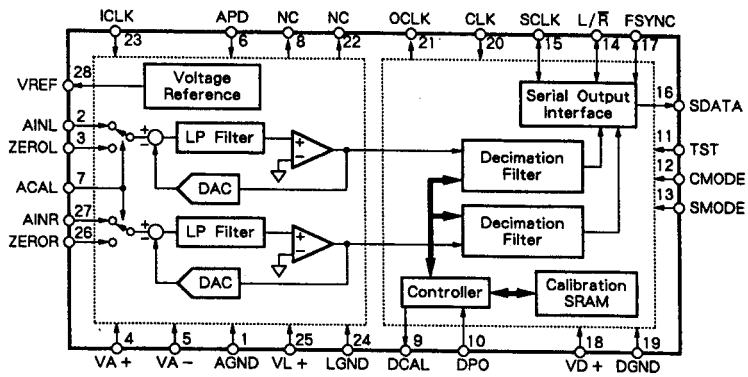
No.	Name	I/O	Function	No.	Name	I/O	Function
1	P/S	I	Serial and parallel controls switch.	19	MCK	O	System clock output.
2	RZ	O	R ch digital zero detection output.	20	LATCH (EMI)	I	Data latch signal input pin for attenuator when controlling with serial. Deemphasis filter mode selection pin when controlling with parallel.
3	TEST	I	Test pin. Normally, used to "H".				
4	VDA	—	Analog power supply voltage for R ch DA converter.				
5	RO	O	R ch data positive output.	21	SHIFT (EM2)	I	Shift clock input pin for attenuator when controlling with serial. Deemphasis filter mode selection pin when controlling with parallel.
6	RO	O	R ch data negative output.				
7	GNDA	—	Analog ground for R ch DA converter.				
8	GNDA	—	Analog ground for L ch DA converter.	22	ATT (MUTE)	I	Data input pin for attenuator when controlling with serial. Muting pin when controlling with parallel. "H" at mute on.
9	LO	O	L ch data negative output.				
10	LO	O	L ch data positive output.				
11	VDA	—	Analog power supply voltage for L ch DA converter.	23	OSCE	I	System clock control. "L" at system clock is stopped .
12	GNDX	—	Ground of oscillation block.	24	RESET	I	Reset pin. Reset the Σ Δ circuit and attenuator data set to 00 (HEX) for "L".
13	XI	I	Connect the crystal. Generate the needful clock for system.				
14	XO	O					
15	VDX	—	Power supply voltage of oscillation block.	25	DATA	I	Data input.
16	GND	—	Ground of logic block.	26	BCK	I	Bit clock input.
17	C	I	Clock selection. "L" is correspond to 256fs and "H" is correspond to 384fs.	27	LRCK	I	LR clock input. ("H" : L ch data)
18	LZ	O	L ch digital zero detection output.	28	VDD	—	Power supply voltage of logic block.

■ CS5339 (IC804)
16 Bit ΔΣ System 2ch A/D Converter

• Pin Functions

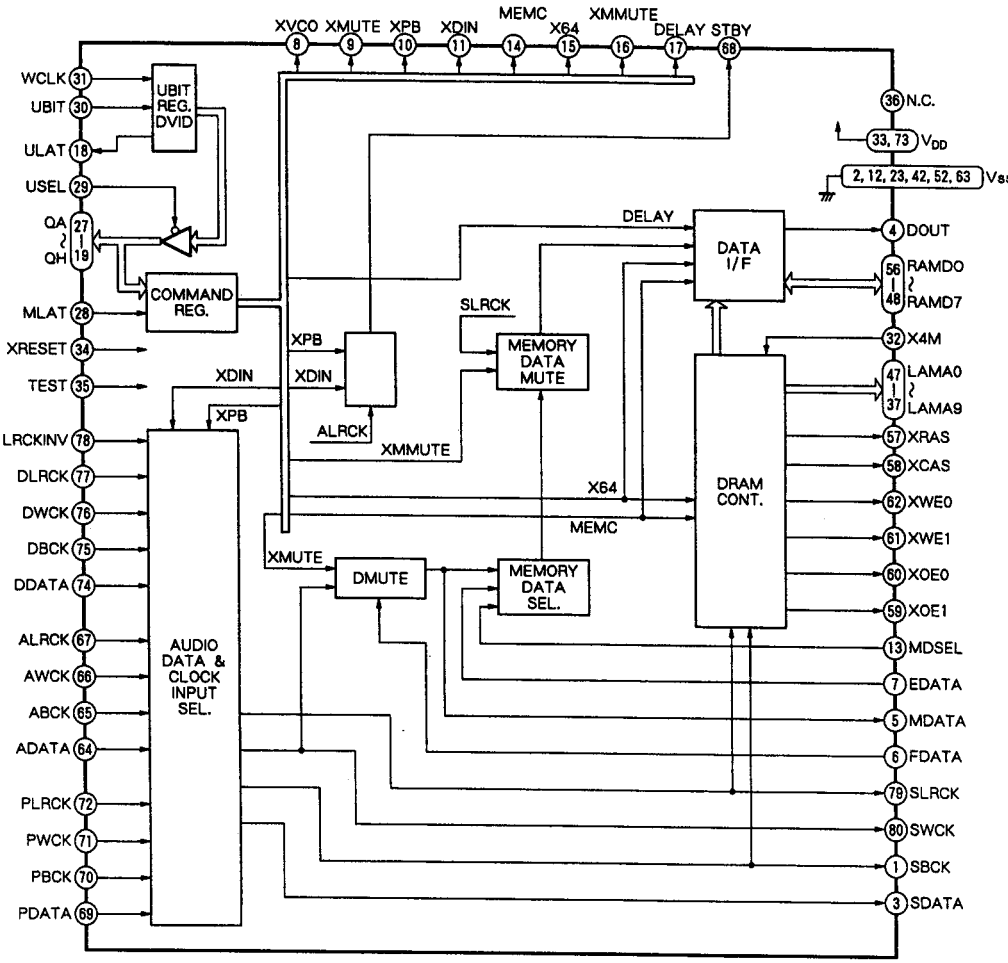
No.	Name	I/O	Function
1	AGND	–	Analog ground pin.
2	AINL	I	L ch analog input pin. Connect a capacitor (10nF) between this pin and AGND pin.
3	ZEROL	I	L ch zero level input pin. Normally, the Lch offset is calibrated using the input voltage of this pin as the zero level. Connect to AGND pin.
4	VA+	–	Analog positive power supply voltage pin, +5V.
5	VA –	–	Analog negative power supply voltage pin, – 5V.
6	APD	I	Power down pin of analog block. Power down mode for "H".
7	ACAL	I	Analog calibration pin. Normally, connect to DCAL pin. Switch the input pin of external signal by this pin's level. "H" : Zero level input pin (ZEROL, ZEROR) "L" : Analog input pin (AINL, AINR)
8	NC	–	No connection. Use for open.
9	DCAL	O	Digital calibration pin. Indicates that offset calibration is in progress. Normally, connect to the ACAL pin. Falls down immediately when a power down signal is input to the DPD pin. DCAL is set to L after a 4096 L/$\overline{R}$ cycle (about 85 ms when fs=48 kHz) from fall down of the DPD pin and indicates the end of calibration.
10	DPD	I	Power down pin of digital block. Goes to power down mode when this pin is H. Offset calibration starts at the falling edge. Always perform calibration after turning the power on or changing the clock frequency.
11	TST	I	Test pin. Connect to DGND pin.
12	CMODE	I	Master clock selection pin. "L" : CLK=256fs (12.288MHz fs=48kHz) "H" : CLK=384fs (18.432MHz fs=48kHz)
13	SMODE	I	Interface clock selection pin. Set the input and output of the L/$\overline{R}$, SCLK and FSYNC clock pins. L : Slave mode (all pins are input pins) H : Master mode (all pins are output pins)
14	L/$\overline{R}$	I/O	Input channel selection pin. Slave mode: Inputs fs clock signals. Outputs the Lch and MSB data at the rising edge and the MSB data of the Rch at the falling edge. Master mode: Outputs fs clock signals. Outputs SDATA after ISCLK at the L/$\overline{R}$ edge. This pin is H during power down (DPD=H).
15	SCLK	I/O	Serial data clock pin. Outputs 1-bit data at the falling down of this pin. Slave mode : Inputs clock signals of 32fs to 64fs. Master mode : Outputs clock signals of 64fs. This pin is L during power down (DPD=H).
16	SDATA	O	Serial data output pin. The data is output from MSB in order in 2s complementary form. After 16-bit output, the 3-bit over/under scale flag and L/R flag are output. This is L during power down (DPD=H).
17	FSYNC	I/O	Frame sync. clock pin. Slave mode : When FSYNC is H, SDATA output is enabled. Master mode : Outputs 2fs clock signals. When 16-bit data is being output, FSYNC is H. This can be used for data latch. FSYNC is L during power down (DPD=H).
18	VD+	–	Digital power supply voltage, +5V.
19	DGND	–	Digital ground pin.
20	CLK	I	Master clock input pin. CMODE = "H" : 384fs, CMODE = "L" : 256fs
21	OCLK	O	128fs clock output pin. Toggles at the rising of the master clock (CLK). OCLK is L during power down (DPD=H).
22	NC	–	No connection. Use for open.
23	ICLK	I	128fs clock input pin. Clock signal for the analog section. Connect to pin OCLK. The sampling rate of the Δ Σ modulator is 64 fs.
24	LGND	–	Logic ground pin of analog block.
25	VL+	–	Logic power supply voltage pin of analog block, +5V
26	ZEROR	I	R ch zero input pin. Normally, the Rch offset is calibrated using the input voltage of this pin as the zero level. Connect to pin AGND.
27	AINR	I	R ch analog input pin. Connect to the 10 nF condenser between this pin and pin AGND.
28	VREF	O	Reference voltage output pin, – 3.68V. The full-scale of the input signals depends on the voltage here. FS= ± 3.68 V when VREF=-3.68 V Connect the 6.8 μF electrolytic condensor and 0.1 μF ceramic condensor between this pin and AGND in parallel.

- **Block Diagram**



■ PD6107A (IC305)
Memory Control IC

- **Block Diagram**



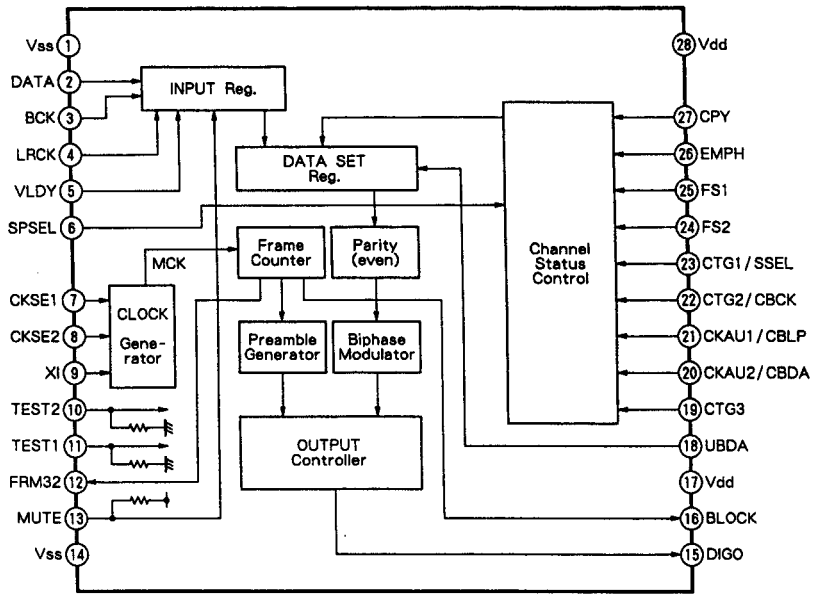
• Pin Functions

No.	Name	I/O	Function
1	SBCK	O	Bit clock output which was selected by input selector.
2	Vss	–	Connect to ground.
3	SDATA	O	Data output which was selected by input selector.
4	DOUT	O	Data output which was delayed by external RAM.
5	MDATA	O	Data output which was through the digital mute.
6	FDATA	O	Data input to digital mute.
7	EDATA	O	Data input to external RAM. Select MDSEL with H.
8	XVCO	O	Output from command register set to QA. Can be used as an general-purpose register.
9	XMUTE	O	Output from command register set to QB. Sets digital mute to ON with L. Normalized at the falling of SWCK.
10	XPB	O	Output from command register set to QC. Selects PLRCK, PWCK, PBCK and PDATA of the input selector with L.
11	XDIN	O	Output from command register set to QD. Effective when XPB is H. Selects DLRCK, DWCK, DBCK or DDATA of the input selector with L, and ALRCK, AWCK, ABCK or ADATA of the input selector with H.
12	Vss	–	Connect to ground.
13	MDSEL	I	Input to select data to be written in external RAM. Selects FDATA passing digital mute with L and EDATA with H.
14	MEMC	O	Output from command register set to QE. Reset signal for the memory controller. Reset with L. The two samplings (8 words) directly after reset are not written in the memory.
15	X64	O	Output from command register set to QF. Select the clock signals for the memory controller. 64 fs at L and 32 fs at H. To be matched to SBCK.
16	XMMUTE	O	Output from command register set to QG. Mute signal of data to be written in memory. Mute ON at L. Normalized at the rising of SLRCK.
17	DELAY	O	Output from command register set to QH. Memory-through control signal. Data passing through the memory is output from DOUT at L (data selected with MDSEL), and data delayed by the memory at H.
18	ULAT	O	Output obtained through 8-division of WCLK at the falling. U-bit data is output to QA through QH at each rising.
19	QH	I/O	MSB (before input) output from U-bit register and data input to command register.
20	QG	I/O	U bit register output and data input to command register.
21	QF		
22	QE		
23	Vss	–	Connect to ground.
24	QD	I/O	U bit register output and data input to command register.
25	QC		
26	QB		
27	QA	I/O	LSB (after input) output from U-bit register and data input to command register.
28	MLAT	I	Input of clock signals for the command register to read. Data set in QA through QH is read at the rising of this signal and output to XVCO, XMUTE, XPB, XDIN, MEMC, X64, XMMUTE and DELAY.
29	USEL	I	Input of QA through QH two-way bus input/output changeover. L : output , H : input
30	UBIT	I	U bit data input. Must be changed with the falling edge of WCLK.
31	WCLK	I	U bit shift clock input .
32	X4M	I	Selection input of memory capacity. L : 4M bits, H : 8M bits.
33	V_{DD}	–	Connect to +5V.
34	XRESET	I	Reset input. Reset for L.
35	TEST	I	Test mode input. Normally, active L.
36	N.C.	–	No connection.
37	RAMA9	O	Address outputs to external RAM.
38	RAMA8		
39	RAMA7		
40	RAMA6		
41	RAMA5		

No.	Name	I/O	Function
42	Vss	–	Connect to ground.
43	RAMA4	O	Address outputs of external RAM.
44	RAMA3		
45	RAMA2		
46	RAMA1		
47	RAMA0		
48	RAMD7	I/O	Data inputs and outputs of external RAM.
49	RAMD6		
50	RAMD5		
51	RAMD4		
52	Vss	–	Connect to ground.
53	RAMD3	I/O	Data inputs and outputs of external RAM.
54	RAMD2		
55	RAMD1		
56	RAMD0		
57	XRAS	O	Low address select output of external RAM.
58	XCAS	O	Column address select output of external RAM.
59	XOE1	O	Output enable output of external RAM. Connect to another external RAM during 8M bit output.
60	XOE0	O	Output enable output of external RAM.
61	XWE1	O	Write enable output of external RAM. Connect to another external RAM during 8M bit output.
62	XWE0	O	Write enable output of external RAM.
63	Vss	–	Connect to ground.
64	ADATA	I	Data input of input selector.
65	ABCK	I	Bit clock input of input selector.
66	AWCK	I	Word clock input of input selector.
67	ALRCK	I	LR clock input of input selector.
68	STBY	O	Standby output of AD converter. Standby mode with H and operation mode with L. Set to L when both XPB and XDIN are H and normalized at the rising of ALRCK.
69	PDATA	I	Data input of input selector.
70	PBCK	I	Bit clock input of input selector.
71	PWCK	I	Word clock input of input selector.
72	PLRCK	I	LR clock input of input selector.
73	V_{DD}	–	Connect to +5V.
74	DDATA	I	Data input of input selector.
75	DBCK	I	Bit clock input of input selector.
76	DWCK	I	Word clock input of input selector.
77	DLRCK	I	LR clock input of input selector.
78	LRCKINV	I	Polarity inverse input of DLRCK. Inverse with L and through with H.
79	SLRCK	O	Output of LR clock selected by input selector.
80	SWCK	O	Output of word clock selected by input selector.

■ TC9231N (IC321)
Digital Interface IC

• Block Diagram

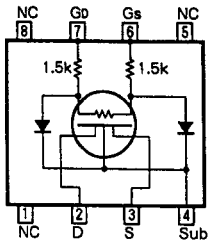


• Pin Function

No.	Name	I/O	Function	Remarks
1	Vss	–	Ground.	
2	DATA	I	Data input.	
3	BCK	I	Bit clock input.	
4	LRCK	I	Clock input of right and left switch.	
5	VLDY	I	Validly flag input. Set to H for corrected data.	
6	SPSEL	I	Input mode setting of channel status bit.	
7	CKSE1	I	Dividing ratio setting for the clock input to XI.	
8	CKSE2			
9	XI	I	Master clock input for operation.	
10	TEST2	I	Test pin. Normally use for "L".	Pull-down
11	TEST1			
12	FRM32	O	Clock output with 32 frames as 1 cycle.	
13	MUTE	I	Mute pin. "L" : internal MUTE ON. "H" : internal MUTE OFF.	Pull-up
14	Vss	–	Ground.	
15	DIGO	O	Output of data converted to digital audio interface format.	
16	BLOCK	O	Clock output with 1 block as 1 cycle.	
17	Vdd	–	Power supply voltage.	
18	UBDA	I	User data input.	
19	CTG3	I	Category code setting.	
20	CKAU2/CBDA	I	Clock precision setting . (SPSEL="H") Serial input of channel status data. (SPSEL="L")	
21	CKAU1/CBLP	I	Clock precision setting . (SPSEL="H") Latch pulse input at serial input of channel status data. (SPSEL="L")	
22	CTG2/CBCK	I	Category code setting. (SPSEL="H") Bit clock input at serial input of channel status data. (SPSEL="L")	
23	CTG1/SSEL	I	Category code setting. (SPSEL="H") Serial input mode selection of channel status data. (SPSEL="L")	
24	FS2	I	Sampling frequency setting of channel status data.	
25	FS1			
26	EMPH	I	Emphasis setting of channel status data.	
27	CPY	I	Copy bit setting of channel status data.	
28	Vdd	–	Power supply voltage.	

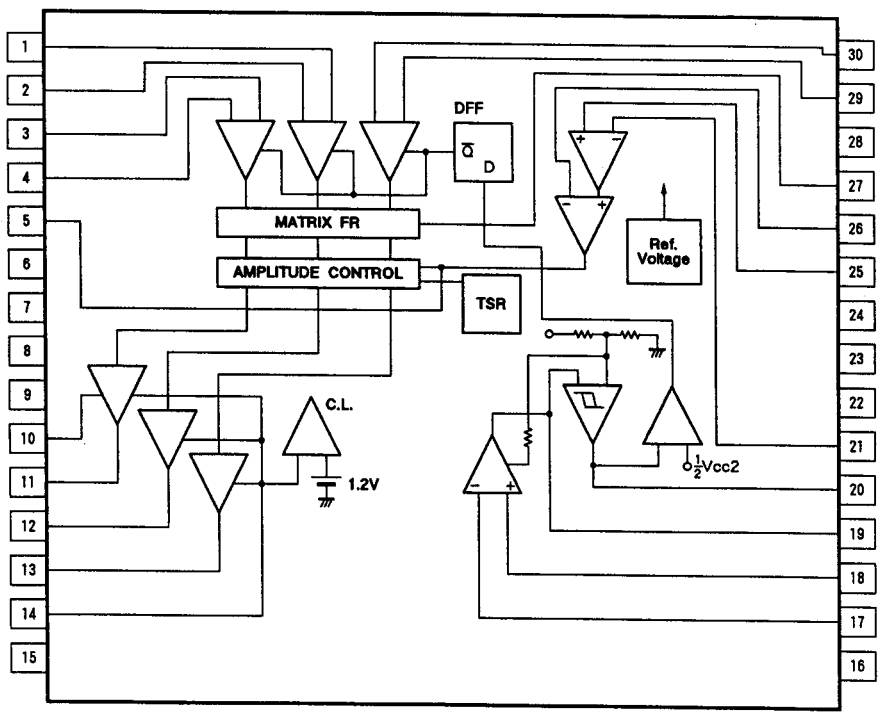
■ CXD7500M (IC102)
Voltage Control Type Variable Resistor

- **Block Diagram**



■ LB1687 (IC108)
Three-phase Brushless Motor Driver

- **Block Diagram**



- **Truth Table**

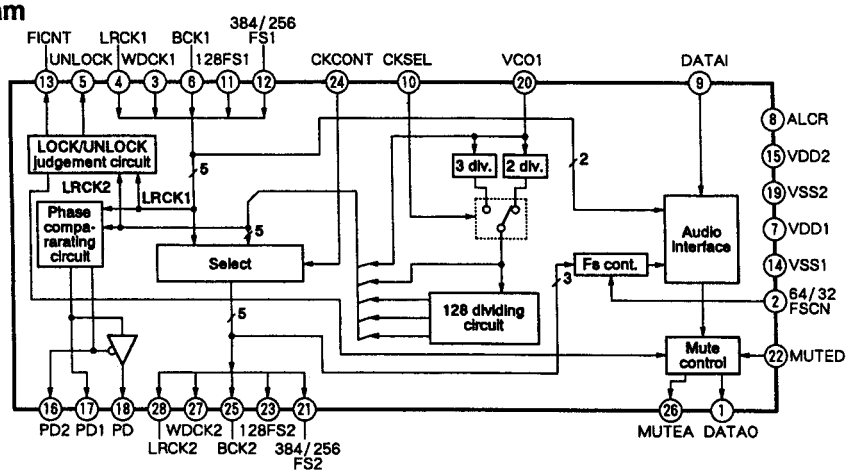
Step No.	Source Sink	Input U	Input V	Input W	Positive • Negative Control F/RC
1	W phase → V phase	H	H	L	L
	V phase → W phase				H
2	W phase → U phase	H	L	L	L
	U phase → W phase				H
3	V phase → W phase	L	L	H	L
	W phase → V phase				H
4	U phase → V phase	L	H	L	L
	V phase → U phase				H
5	V phase → U phase	H	L	H	L
	U phase → V phase				H
6	U phase → W phase	L	H	H	L
	W phase → U phase				H

Input H : Input 1 has a higher electric potential of 0.2 V or more in regard to input 2 for each phase.
L : Input 1 has a lower electric potential of 0.2 V or more in regard to input 2 for each phase.

Positive/negative control H : 2.0 – Vcc2
L : 0 – 0.3V

■ M65811FP (IC315)
Jitter Absorption Data Buffer for Digital Audio

• Block Diagram

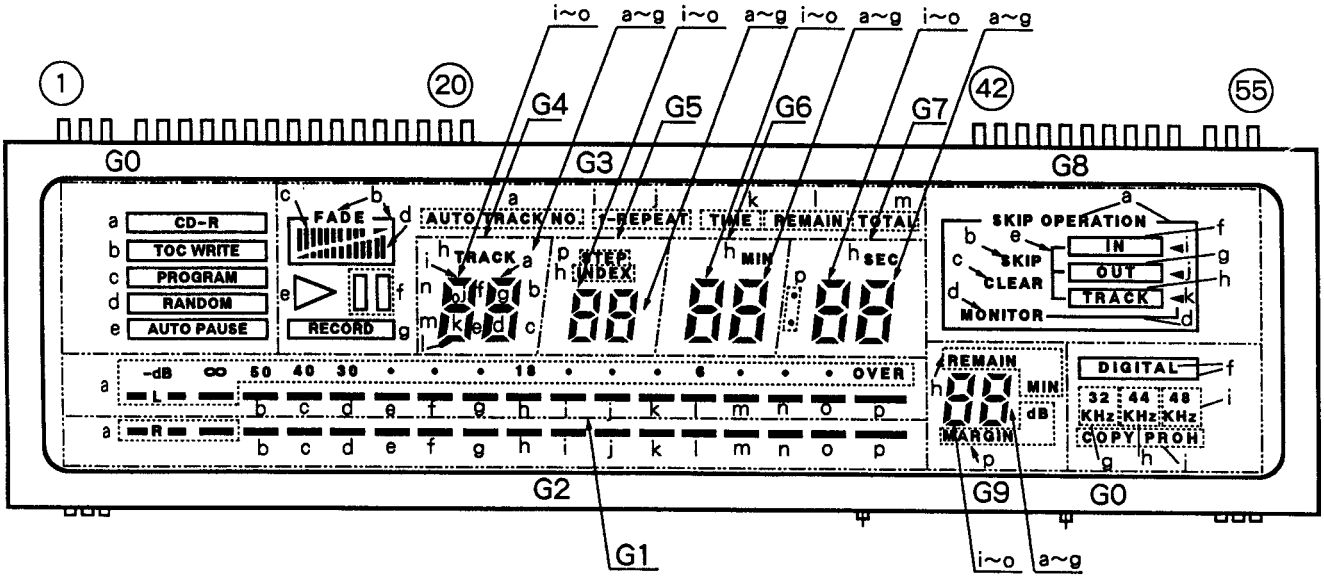


• Pin Functions

No.	Name	I/O	Function
1	DATAO	O	Data output. When pin 24 is H, first system data will out. When pin 24 is L, second system data will out.
2	64/32FSCN	I	Bit clock 64/32 fs switch. Control the data rate of data output. . (L : 64 fs, H : 32 fs)
3	WDCK1	I	First system word clock input. Input 2 fs which generating at first PLL. If its not used, fix to L or H.
4	LRCK1	I	First system LR clock input. Input 1 fs which generating at first PLL. This signal is certain to input.
5	UNLOCK	O	Unlock. H is output when a mismatch in synchronizing the 1st PLL system clock and 2nd PLL system clock occurs.
6	BCK1	I	First system bit clock input. Input 64 fs which generating at first PLL. This signal is certain to input.
7	V_{DD}	–	Power supply voltage 1 for internal logic and I/O.
8	ALCR	I	Reset. Reset signal input. (L : reset)
9	DATAI	I	Data input. Input data with MSB first synchronizing with 64 fs.
10	CKSEL	I	Master clock selection. Select with oscillation frequency of VCXO. (L : 256f s, H : 384 fs)
11	128FS1	I	First system 128 fs clock input. Input 128 fs which generating at first PLL. If its not used, fix to L or H.
12	384/256FS1	I	First system 384/256 fs clock input. Input 256 fs or 384 fs which generating at first PLL. If its not used, fix to L or H.
13	FICNT	O	90-phase aberration detection. When the aberration of the 1st system LR clock and 2nd system LR clock is greater than 90-, a L level signal is output.
14	Vss1	–	Ground 1 for internal logic or I/O.
15	V_{DD2}	–	Power supply voltage 2 for phase comparating output.
16	PD2	O	Phase comparating output of phase detection 2. (Connect to enable of external 3 state.)
17	PD1	O	Phase comparating output of phase detection 1. (Connect to enable of external 3 state.)
18	PD	O	Phase comparating output of phase detection. (Internal 3 state output.)
19	Vss2	–	Ground 2 for phase comparating output.
20	VCOI	I	Master clock input. Input master clock from external VCXO.
21	384/256FS2	O	384/256 fs clock output. When pin 24 is H, first system 384/256 fs clock will out. When pin 24 is L, second system 384/256 clock will out.
22	MUTED	I	Forced mute input. Forced mute of second system data. (H : Mute ON, L : Mute OFF)
23	128FS2	O	128f s clock output. When pin 24 is H, first system 128 fs bit clock will out. When pin 24 is L, second system 128 fs clock will out.
24	CKCONT	I	First / Second system select. Switch the first or second systems clock output. (L : Second system, H : First system) Data output is in the same manner.
25	BCK2	O	Bit clock output. When pin 24 is H, first system bit clock will out. When pin 24 is L, second system bit clock will out.
26	MUTEA	O	External system mute output. Mute control signal output to external system. (H : Mute ON, L : Mute OFF)
27	WDCK2	O	Word clock output. When pin 24 is H, first system word clock will out. When pin 24 is L, second system word clock will out.
28	LRCK2	O	LR clock output. When pin 24 is H, first system LR clock will out. When pin 24 is L, second system LR clock will out.

8. FL INFORMATION

• FL DISPLAY (V701)



• PIN ASSIGNMENT

Pin No.	Assignment	Pin No.	Assignment
1	F	29	NP
2	F	30	NP
3	F	31	NP
4	NP	32	NP
5	a	33	NP
6	b	34	NP
7	c	35	NP
8	d	36	NP
9	e	37	NP
10	f	38	NP
11	g	39	NP
12	h	40	NP
13	i	41	NP
14	j	42	G9
15	k	43	G8
16	l	44	G7
17	m	45	G6
18	n	46	G5
19	o	47	G4
20	p	48	G3
21	NP	49	G2
22	NP	50	G1
23	NP	51	G0
24	NP	52	NP
25	NP	53	F
26	NP	54	F
27	NP	55	F
28	NP		

F:Filament G0~G9:Grid
a~p:Anode NP:No pin

• ANODE GRID ASSIGNMENT & PIN ASSIGNMENT

	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9
a	CD-R	-dB L 数字 ∞	R	AUTO TRACK NO.	a	a	a	a	SKIP OPERATION	a
b	TOC WRITE	-50dB	-50dB	FADE	b	b	b	b	SKIP	b
c	PROGRAM	-40dB	-40dB		c	c	c	c	CLEAR	c
d	RANDOM	-30dB	-30dB		d	d	d	d	MONITOR	d
e	AUTO PAUSE	-27dB	-27dB	▷	e	e	e	e	E	e
f	DIGITAL	-24dB	-24dB	▯▯	f	f	f	f	IN	f
g	32 kHz	-21dB	-21dB	RECORD	g	g	g	g	OUT	g
h	44 kHz	-18dB	-18dB		TRACK	INDEX	MIN	SEC	TRACK	REMAIN MIN
i	48 kHz	-15dB	-15dB	1 –	i	i	i	i	◀ (IN)	i
j	COPY PROH	-12dB	-12dB	REPEAT	j	j	j	j	◀ (OUT)	j
k		-09dB	-09dB	TIME	k	k	k	k	◀ (TRACK)	k
l		-06dB	-06dB	REMAIN	l	l	l	l		l
m		-04dB	-04dB	TOTAL	m	m	m	m		m
n		-02dB	-02dB		n	n	n	n		n
o		-00dB	-00dB		o	o	o	o		o
p		OVER	OVER			STEP		:		dB MARGIN

9. ADJUSTMENTS

1. Adjustment Methods

If a compact disc recorder is adjusted incorrectly or inadequately, it may malfunction or not work at all even though there is nothing at all wrong with the pickup or the circuitry. Adjust correctly following the adjustment procedure.

● Measuring Instruments and Tools

1. Dual trace oscilloscope (10 : 1 probe)
2. Low-frequency oscillator
3. Test disc (YEDS-7)
4. Low pass filter (39kΩ +0.001 μF), (560kΩ +0.047 μF)
5. Resistor (100 kΩ)
6. Hexagonal screwdriver (1.5mm diagonal)
7. Standard tools
8. Optical power meter
9. Small screwdriver

● Adjustment Items/Verification Items and Order

Adjustment 1

Step	Item	Test Point	Adjustment Location
1	Playback power adjustment	Objective lens of pickup	VR103 (PB. PW)
2	Coarse focus offset adjustment	TP201, Pin 6 (FCS ERR)	VR105 (FE. OFS)
3	Coarse skew adjustment	TP201, Pin 1 (RF)	Radial tilt adjustment screw and Tangential tilt adjustment screw
4	Grating adjustment	TP2, Pin 5 (TF)	Grating adjustment slit
5	DPP (tracking offset) adjustment	TP2, Pin 5 (TF)	VR112 (TE. OFS)
6	Fine skew adjustment	TP201, Pin 1 (RF)	Radial tilt adjustment screw and Tangential tilt adjustment screw
7	Grating re-adjustment	TP2, Pin 5 (TE)	Grating adjustment slit

Adjustment 2

Step	Item	Test Point	Adjustment Location
1	Slider speed control offset adjustment	TP1, Pin 7 (SLDDRV)	VR101 (SLD. OFS)
2	Sample pulse phase adjustment	TP1, Pin 3 (EFM) TP1, Pin 4 (XSAMPLE)	VR102 (SMPL. OLY)
3	Playback power re-adjustment	Objective lens of pickup	VR103 (PB. PW)
4	Recording power adjustment	Objective lens of pickup	VR104 (REC. PW)
5	Focus offset adjustment	TP201, Pin 6 (FCSER)	VR105 (FE. OFS)
6	RF offset adjustment	TP201, Pin 1 (RF)	VR106 (RF. OFS)
7	WBL + offset adjustment	TP2, Pin 8 (RWBL)	VR107 (WBL+. OFS)
8	WBL offset adjustment	TP2, Pin 7 (WBL)	VR108(WBL. OFS)
9	Main and Sub mix ratio a djustment	TP2, Pin 3 (STE) TP2, Pin 4 (MSTE)	VR110 (MS. MIXRATE)
10	Tracking amp. gain adjustment	TP2, Pin 5 (TE)	VR111 (TE. GAIN)
11	Tracking offset adjustment	TP2, Pin 5 (TE)	VR112 (TE. OFS)
12	Fine focus offset adjustment	TP201, Pin 1 (RF)	VR105 (FE. OFS)
13	Focus servo loop gain adjustment	TP201, Pin 5 (FCSIN) TP201, Pin 6 (FCSER)	VR201 (FCS. GAIN)
14	Tracking servo loop gain adjustment	TP201, Pin 2 (TRKER) TP201, Pin 3 (TRKIN)	VR202 (TRK. GAIN)

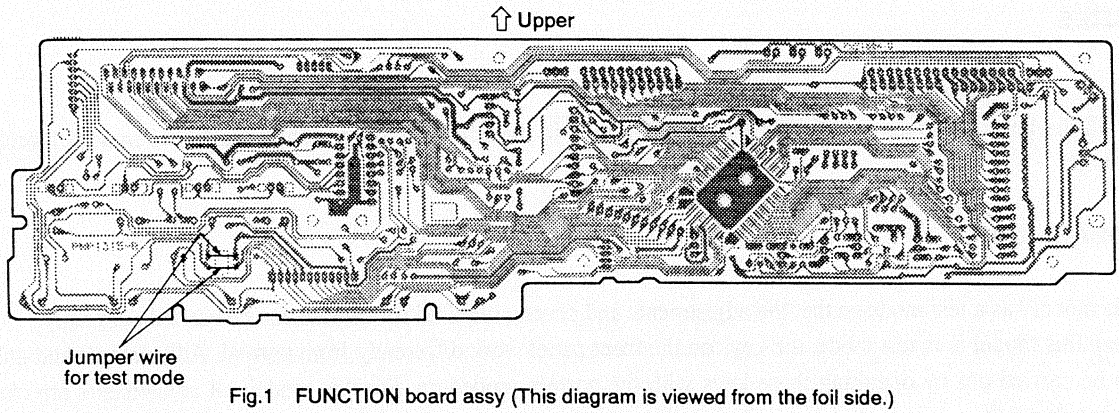


Fig.1 FUNCTION board assy (This diagram is viewed from the foil side.)

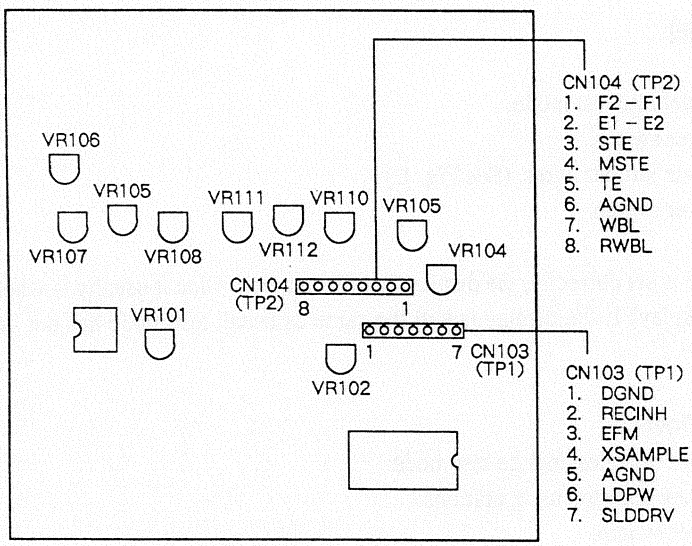


Fig.2 HEAD board assy

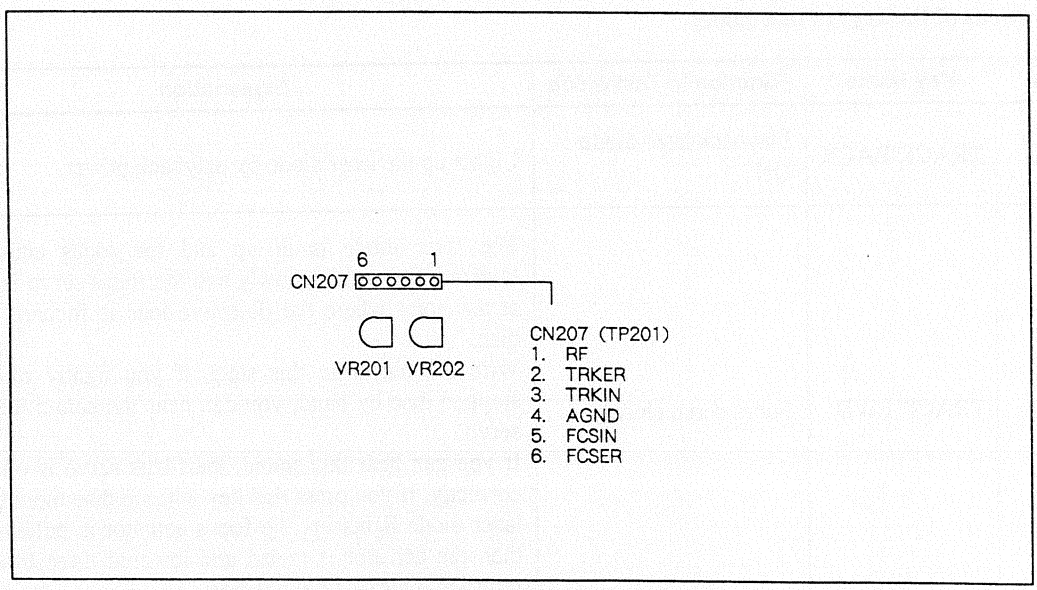


Fig.3 SERVO•DIGITAL board assy

● Notes

1. Use a 10:1 probe for the oscilloscope.
2. All the knob positions (settings) for the oscilloscope in the adjustment procedures are for when a 10:1 probe is used.

● Test Mode

This model has a test mode so that the adjustments and checks required for service can be carried out easily.
When this model is in test mode, the keys on the front panel work differently from normal. Adjustments and checks can be carried out by operating these keys with the correct procedure. For this model, all adjustments are carried out in test mode.

[Setting to Test Mode]

How to set this model into test mode.
1. Turn off the power switch.
2. Short the test mode jumper wires. (See Fig. 1.)
3. Turn on the power switch.

When the test mode is set correctly, the display is different from what it usually is when the power is turned on. (lights up all FL display) If the display is still the same as usual, test mode has not been set correctly, so repeat Steps 1 − 3.

[Release from Test Mode]

Here is the procedure for releasing the test mode:
1. Press the STOP key and stop all operations.
2. Turn off the power switch.

[Operations of the keys in test mode]

Code	Key Name	Function In Test Mode	Explanation
⏮	TRACK BACK	Playback laser diode ON	Lights up the laser diode by playback power.
⏭	TRACK FWD	Focus servo closes	The laser diode is lit up and the focus actuator is lowered, then raised slowly and the focus servo is closed at the point where the objective lens is focused on the disc. With the player in this state, if you lightly rotate the stopped disc by hand, you can hear the sound the focus servo. If you can hear this sound, the focus servo is operating correctly. If you press this key with no disc mounted, the laser diode lights up, the focus actuator is pulled down, then the actuator is raised and lowered three times and returned to its original position.

Code	Key Name	Function In Test Mode	Explanation
▷	PLAY	Spindle servo ON	Starts the spindle motor in the clockwise direction and when the disc rotation reaches the prescribed speed (about 500 rpm at the inner periphery), sets the spindle servo in a closed loop.
▯▯	PAUSE	Tracking servo close/open	Pressing this key when the focus servo and spindle servo are operating correctly in closed loops puts the tracking servo into a closed loop, displays the track number being played back and the elapsed time on the front panel, and outputs the playback signal. If the elapsed time is not displayed or not counted correctly or the audio is not played back correctly, it may be that the laser is shining on the section with no sound recorded at the outer edge of the disc, that something is out of adjustment, or that there is some other problem. This key is a toggle key and open/close the tracking servo alternately. This key has no effect if no disc is mounted.
◁◁	MANUAL SEARCH REV	Carriage reverse (inwards)	Moves the pickup position toward the inner diameter of the disc. When this key is pressed with the tracking servo in a closed loop, the tracking servo automatically goes into an open loop. Since the motor does not automatically stop at the mechanical end point in test mode, be careful with this operation.
▷▷	MANUAL SEARCH FWD	Carriage forward (outwards)	Moves the pickup position toward the outer diameter of the disc. When this key is pressed with the tracking servo in a closed loop, the tracking servo automatically goes into an open loop. Since the motor does not automatically stop at the mechanical end point in test mode, be careful with this operation.
□	STOP	Stop	Initializes and the disc rotation stops. The pickup and disc remain where they are when this key is pressed.
⏏	OPEN/CLOSE	Disc tray open/close	Open/close the disc tray. This key is a toggle key and open/close tray alternately. Pressing this key when the disc is turning stops the disc, then opens the tray. This key operation does not affect the position of the pickup.
○ ↓ ◎	REC ↓ REC MUTE	Maximum recording power. Laser diode ON.	Lights up the laser diode with maximum recording power and normal EFM by pressing REC and REC MUTE keys in order. * The laser diode may be damaged if adjustments are made before pressing these keys.

[How to play back a disc in test mode]

In test mode, since the servos operate independently, playing back a disc requires that you operate the keys in the correct order to close the servos.
Here is the key operation sequence for playing back a disc in test mode.

TRACK FWD ▷▷|	Lights up the laser diode and closes the focus servo.
⇩	
PLAY ▷	Starts the spindle motor and closes the spindle servo.
⇩	
PAUSE ▯▯	Closes the tracking servo.

Wait at least 2-3 seconds between each of these operations.

1. Playback Power Adjustment

Adjustment 1

● Objective	To optimize the playback power of the laser diode.		
● Symptom when out of adjustment	Play does not start, track search is impossible, track are skipped.		
● Measurement instrument connections	Shine the light dischrged from the objective lens on the light power meter sensor. [Settings] Wavelength 790mm Average mode	● Player state ● Adjustment location ● Disc	Test mode, Playback laser diode ON VR103 (PB. PW) None needed

[Procedure]

1. Move the pickup to the outer edge of the disc with the MANUAL SEARCH FWD ▷▷ key.
2. Lights up the playback laser diode by TRACK BACK |◁◁ key.
3. Shine the light discharged from the objective lens in the pickup on the light power meter sensor. Adjust VR103 (PB.PW) so that the playback laser diode output is an average 0.6 mW ± 0.05 mW.

* Recording on the disc is not possible in test mode.

2. Coarse Focus Offset Adjustment

Adjustment 1

● Objective	To coarse adjust the DC offset voltage of the focus servo circuit for perform the tracking and slider adjustments correctly.		
● Symptom when out of adjustment	The model does not focus in, sound broken and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 6 (FCSERR) (Servo • digital board assy) [Settings] 1 mV/division 10 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR105 (FE. OFS) YEDS-7

[Procedure]

1. Adjust VR105 (FE. OFS) so that the DC voltage at TP201, Pin 6 (FCSER) is 0 ± 10mV .

3. Coarse Skew Adjustment

Adjustment 1

● Objective	To coarse adjust the angle to the disc of pickup for perform the grating and DPP (tracking offset) adjustments correctly.		
● Symptom when out of adjustment	Sound broken, some discs can be played but not others.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 1 (RF). (Servo • digital board assy) [Settings] 20 mV/division 200 ns/division AC mode	● Player state ● Adjustment location ● Disc	Test mode, play Radial adjustment screw and tangential adjustment screw YEDS-7

[Procedure]

1. Move the pickup to the position where the radial/tangential adjustment screws will be seen with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys so that the radial/tangential adjustment screws can be adjusted.
   Press the TRACK FWD ▷▷| key, then the PLAY ▷ key in that order to close the spindle servo.
2. Adjust the RAD (radial direction) and TAN (tangential direction) adjustment acrews alternately with hexagonal screwdriver (1.5 mm) to maximize the RF output at TP201 pin 1.

Note : Radial and tangential mean the direction relative to the disc shown in Fig. 4.

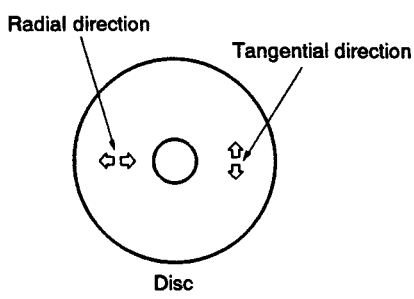
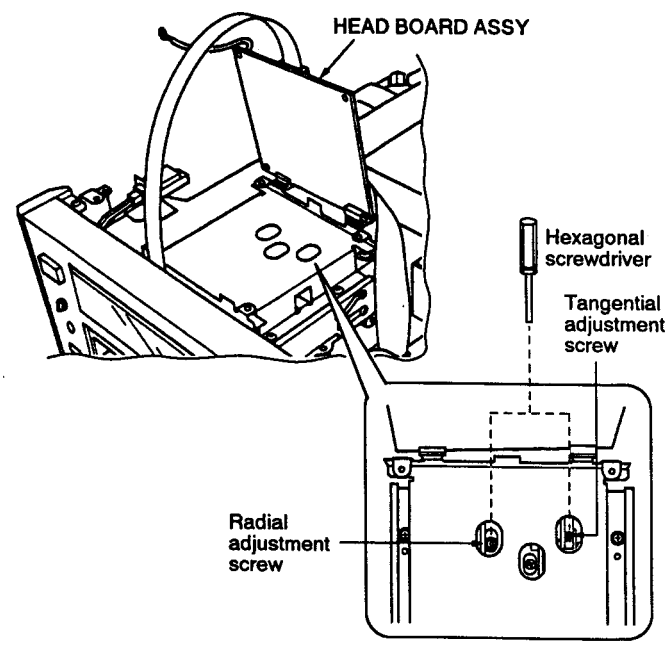


Fig. 4



4. Grating Adjustment

Adjustment 1

● Objective	To align the tracking error generation laser beam spots to the optimum angle on the track.		
● Symptom when out of adjustment	Play does not start, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to TP2, Pin 5 (TE) via a low pass filter. (see Fig. 5) [Settings] 50 mV/division 5 ms/division DC mode	● Player state	Test mode, focus and spindle servos closed and tracking servo open
		● Adjustment location	Grating slit on pickup
		● Disc	YEDS-7

[Procedure]

1. Move the pickup to the position where the grating adjustment slit will be seen with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys so that the grating adjustment can be adjusted.
2. Press the TRACK FWD ▷▷▯ key, then the PLAY ▷ key in that order to close the focus servo then the spindle servo.
3. Insert a screwdriver into the grating adjustment slit and adjust the grating to find the null point.
   For more details, see next page.
4. If you slowly turn the screwdriver clockwise from the null point, the amplitude of the wave gradually increases, then if you continue turning the screwdriver, the amplitude of the wave becomes smaller again. Turn the screw driver counterclockwise from the null point and set the grating to the first point where the wave amplitude reaches its maximum.
   Reference : Fig.6 shows the relation between the angle of the tracking beam with the track and the waveform.
5. Return the pickup to more or less midway across disc with the MANUAL SEARCH REV ◁◁ key, press the PAUSE ▯▯ key and check that the track number and elapsed time are displayed on the front panel. If they are not displayed at this time or the elapsed time changes irregularly, check the null point and adjust the grating again.

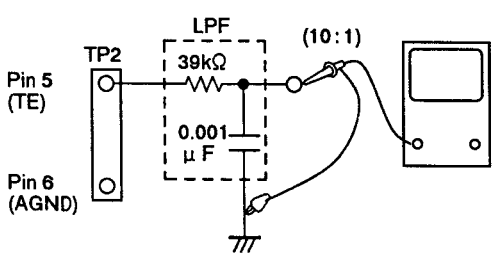
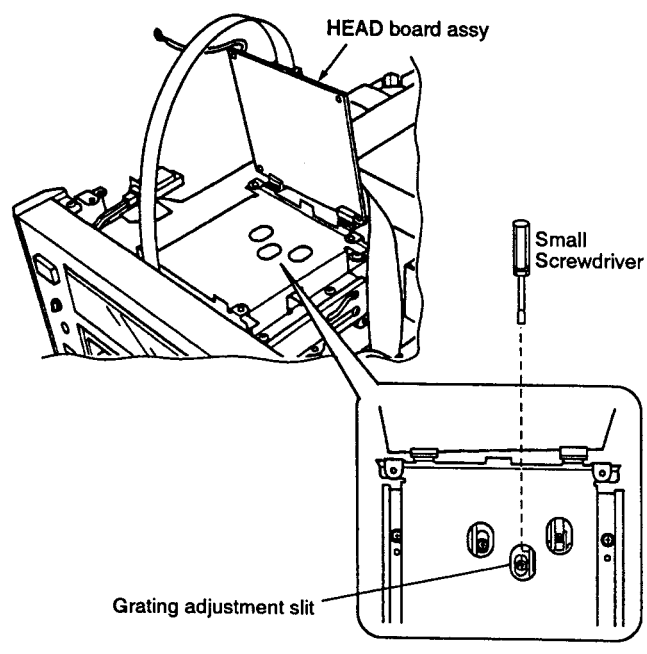


Fig. 5



[How to find the null point]

When you insert the small screwdriver into the slit for the grating adjustment and change the grating angle, the amplitude of the tracking error signal at TP2, Pin 5 changes. Within the range for the grating, there are five or six locations where the amplitude of the wave reaches a minimum. Of these five or six locations, there is only one at which the envelope of the waveform is smooth. This location is where the three laser beams divided by the grating are all right above the same track. (See Fig. 6.)

This point is called the null point. When adjusting the grating, this null point is found and used as the reference position.

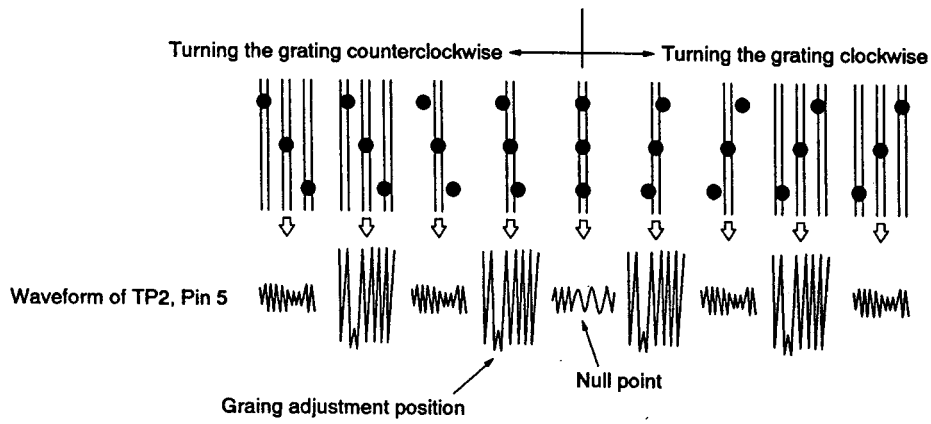
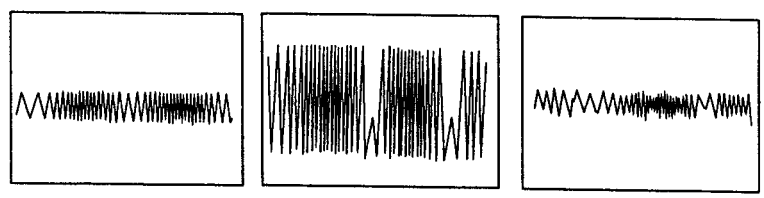


Fig. 6



Note : If the difference between the amplitude of the error signal at the innermost edge and outermost edge of the disc is more than 10%, adjust the grating again.

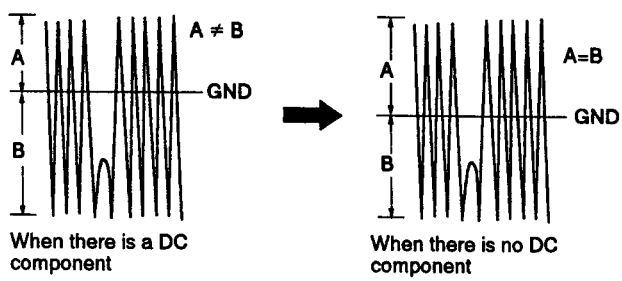
5. DPP (Tracking Offset) Adjustment

Adjustment 1

● Objective	To correct for the variation in the sensitivity of the tracking photodiode.		
● Symptom when out of adjustment	Play does not start or track search is impossible.		
● Measurement instrument connections	Connect the oscilloscope to TP2, Pin 5 (TE) [This connection may be via a low pass filter (39kΩ +0.001 μF).] [Settings] 50 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open VR112 (TE. OFS) YEDS-7

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys.
2. Press the TRACK FWD ▷▷| key, then the PLAY ▷ key in that order to close the focus servo then the spindle servo.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR112 (TE. OFS) so that the positive amplitude and negative amplitude of the tracking error signal at TP2, Pin 5 (TE) are the same (in other words, so that there is no DC component).



When there is a DC component

When there is no DC component

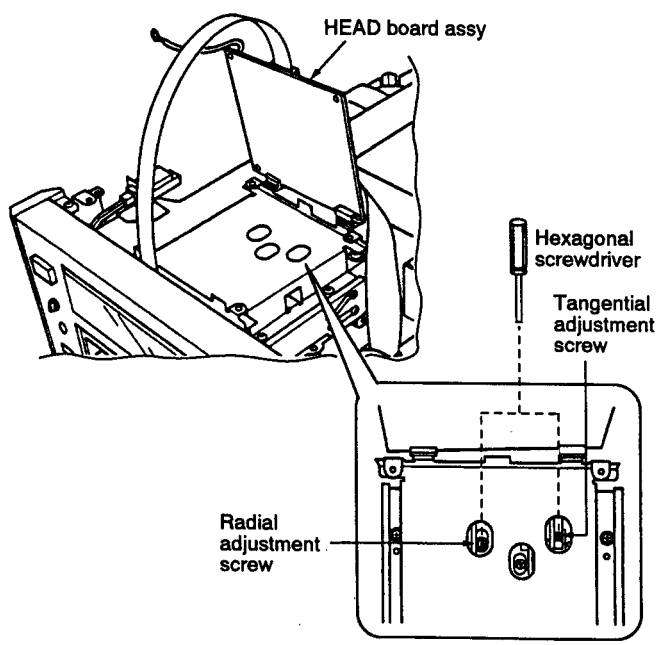
6. Fine Skew Adjustment

Adjustment 1

● Objective	To adjust the angle of the pickup relative to the disc so that the laser beams are shone straight down into the disc for the best read out of the RF signals.		
● Symptom when out of adjustment	Sound broken, some discs can be played but not others.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 1 (RF). (Servo • digital board assy) [Settings] 20mV/division 200ns/division AC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open Pickup radial adjustment screw and tangential adjustment screw YEDS-7

[Procedure]

1. Move the pickup to the position where the radial/tangential adjustment screws will be seen with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys so that the radial/tangential adjustment screws can be adjusted.
   Press the TRACK FWD ▷▷| key, then the PLAY ▷ key in that order to close the focus servo then the spindle servo.
2. First, adjust the radial adjustment screw with the hexagonal screwdriver so that the eye pattern (the diamond shape at the center of the RF signal) can be seen the most clearly.
3. Next, adjust the tangential adjustment screw with the hexagonal screwdriver so that the eye pattern can be seen the most clearly (Fig. 7).
4. Adjust the radial adjustment screw and the tangential adjustment screw again so that the eye pattern can be seen the most clearly. As necessary, adjust the two screws alternately so that the eye pattern can be seen the most clearly.



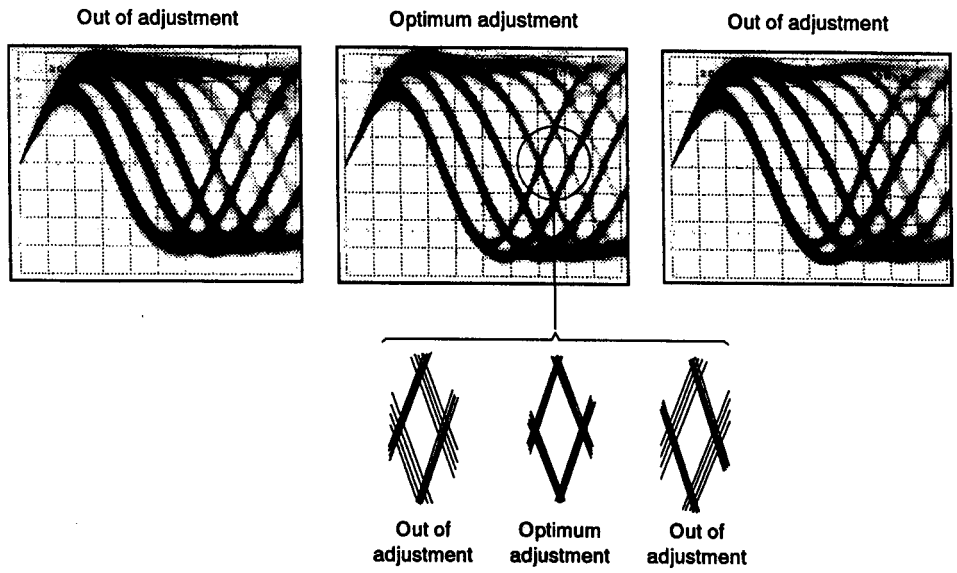


Fig.7 Eye pattern

7. Grating Re-Adjustment

Adjustment 1

Adjust in the same manner as "4. Grating Adjustment" in Adjustment 1.

1. Slider Speed Control Offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the slider speed control amp.		
● Symptom when out of adjustment	Player does not playback (slider moves at stop).		
● Measurement instrument connections	Connect the oscilloscope to TP1, Pin 7 (SLDDRV). GND : TP1, Pin 5 (AGND) [This connection may be via a low pass filter (560k Ω +0.047 μF)] [Settings] 1 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR101 (SLD. OFS) None needed

[Procedure]

1. Move the pickup to midway across the disc with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys.
2. If the pickup (slider) continues moving even when you try to stop it, coarse adjust VR101 (SLD.OFS) to stop it.
3. Adjust VR101 (SLD.OFS) so that the DC voltage at TP1, pin 7 (SLDDRV) is 0 ± 10 mV.
4. Check that pickup (slider) movement is stopped.
   Perform adjustments from step 1 again if the pickup (slider) can move naturally.

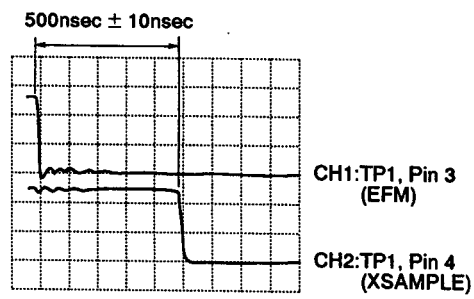
2. Sample Pulse Phase Adjustment

Adjustment 2

● Objective	To optimize the phase of the sampling pulses necessary for the servo during recording.		
● Symptom when out of adjustment	Player does not record nor playback self-recorded discs and skips tracks. (No problems during CD playback)		
● Measurement instrument connections	Connect the oscilloscope to CH1 : TP1, Pin 3 (EFM) CH2 : TP1, Pin 4 (XSAMPLE). GND : TP1, Pin 1 (DGND) [Settings] CH 1 : 0.2 V/division 100 ns/division DC mode CH 2 : 0.2 V/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR102 (SMPL. OLY) None needed

[Procedure]

1. Fully turn VR104 counterclockwise to reduce the power to the minimum.
2. Press the REC ○ key, then the REC MUTE ◎ key.
3. Adjust VR102 (SMPL.OLY) so that the time from the falling edge of TP1, pin 3 (EFM) to the faling edge of TP1, pin 4 (XSAMPLE) is 500 nsec ±10 nsec.



3. Playback power Re-Adjustment

Adjustment 2

Adjust in the same manner as "1. Playback Power Adjustment" in Adjustment 1.

4. Recording Power Adjustment

Adjustment 2

● Objective	To optimize the recording power of the laser diode.		
● Symptom when out of adjustment	The player does not record nor playback self-recorded discs. It also skips tracks and the RF waveform is dirty. (No problems during CD playback)		
● Measurement instrument connections	Shine the light discharged from the objective lens on the light power meter sensor. [Settings] Wavelength 790 nm Average mode	● Player state ● Adjustment location ● Disc	Test mode, maximum recording power ON VR104 (REC. PW) None needed

[Procedure]

1. Fully turn VR104 (REC.PW) counterclockwise to reduce the power to the minimum.
2. Move the pickup to the outer edge of the disc with the MANUAL SEARCH FWD ▷▷ key.
3. Press REC ○ and REC MUTE ⏀ keys in that order to lights up the laser diode.
4. Shine the light discharged from the objective lens in the pickup on the light power meter sensor and adjust VR104 (REC.PW) so that the playback laser diode output is an average of 5.3 mW ± 0.05 mW.

Notes

- Power more than ten times greater than playback power is released during these adjustments. Never look directly at the objective lens.
- The laser diode may be damaged if the recording power is greater than the specified value. Always perform step 1 before making adjustments and be careful not to exceed the specified value in step 4.

5. Focus Offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the focus error amp.		
● Symptom when out of adjustment	The player does not focus in and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 6 (FCSER). (Servo • digital board assy) [Settings] 1 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR105 (FE. OFS) None needed

[Procedure]

1. Adjust VR105 (FE. OFS) so that the DC voltage at TP201, Pin 6 (FCSER) is 0 ± 10mV.

6. RF Offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the RF amp.		
● Symptom when out of adjustment	The player does not focus in and sound broken.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 1 (RF). (Servo•digital board assy) [Settings] 1 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR106 (RF. OFS) None needed

[Procedure]

1. Adjust VR106 (RF. OFS) so that the DC voltage at TP201, Pin 1 (RF) is 0 ± 10mV.

7. WBL+ Offset Adjustment

Adjustment 2

● Objective	To adjust the gain balance of the wobble signal.		
● Symptom when out of adjustment	CD-R disc does not record and playback.		
● Measurement instrument connections	Connect the oscilloscope to TP2, Pin 8 (RWBL). [Settings] 1 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR107 (WBL +. OFS) None needed

[Procedure]

1. Turn VR108 (WBL. OFS) to fully counterclockwise.
2. Adjust VR107 (WBL+. OFS) so that the DC voltage at TP2, Pin 8 (RWBL) is - 10mV ± 10mV.

8. WBL Offset Adjustment

Adjustment 2

● Objective	To optimize the DC offset voltage of the wobble amp.		
● Symptom when out of adjustment	CD-R disc does not record and playback.		
● Measurement instrument connections	Connect the oscilloscope to TP2, Pin 7 (WBL). [Settings] 1 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, stop VR108 (WBL. OFS) None needed

[Procedure]

1. Adjust VR108 (WBL. OFS) so that the DC voltage at TP2, Pin 7 (WBL) is 0 ± 40mV.

9. Main and Sub Mix Ratio Adjustment

Adjustment 2

● Objective	To mix the gain of the main signal output and sub signal output of the pickup.		
● Symptom when out of adjustment	Player does not playback.		
● Measurement instrument connections	Connect the oscilloscope to CH1 : TP2, Pin 3 (STE) CH2 : TP2, Pin 4 (MSTE). [Settings] CH 1 : 50 mV/div. AC mode 10 ms/div. ADD mode CH 2 : 100 mV/div. AC mode	● Player state ● Adjustment location ● Disc	Test mode VR110 (MS. MIXRATE) YEDS-7

[Procedure]

1. Press the TRACK FWD ▷▷| key, then the PLAY ▷ key in that order to close the focus servo then the spindle servo.
2. Set the oscilloscope to ADD mode (waveform adding mode of CH1 and CH2) and observe the adding waveform of CH1 and CH2.
3. Adjust VR110 (MS. MIXRATE) so that the amplitude of waveform becomes minimum.

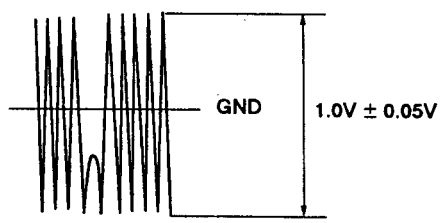
10. Tracking Amp. Gain Adjustment

Adjustment 2

● Objective	To correct the discrepancy in the tracking error level with the pickup.		
● Symptom when out of adjustment	Player does not playback, track search is impossible, tracks are skipped.		
● Measurement instrument connections	Connect the oscilloscope to TP2, Pin 5 (TE). [This connection may be via a low pass filter (39kΩ +0.001 μF).] [Settings] 20 mV/division 5 ms/division DC mode	● Player state ● Adjustment location ● Disc	Test mode, focus and spindle servos closed and tracking servo open VR111 (TE. GAIN) YEDS-7

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys.
2. Press the TRACK FWD ▷▷| key, then the PLAY ▷ key in that order to close the focus servo then the spindle servo.
3. Line up the bright line (ground) at the center of the oscilloscope screen and put the oscilloscope into DC mode.
4. Adjust VR111 (TE. GAIN) so that the positive amplitude and negative amplitude of the tracking error signal at TP2, Pin 5 (TE) is 1.0V ± 0.05V.



11. Tracking Offset Adjustment

Adjustment 2

Adjust in the same manner as "5. DPP Adjustment" in Adjustment 1.

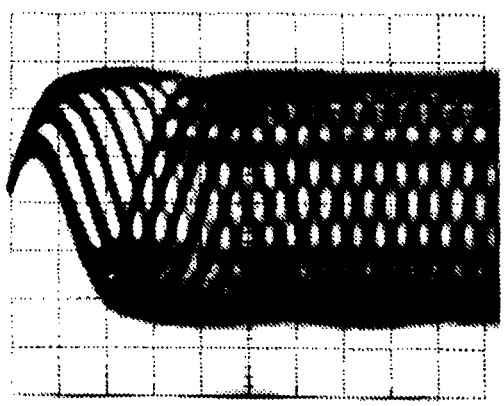
12. Fine Focus Offset Adjustment

Adjustment 2

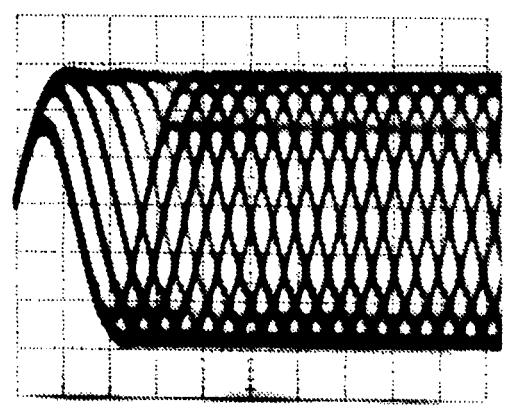
● Objective	To optimize the DC offset voltage of the focus servo circuit.		
● Symptom when out of adjustment	The player does not focus in, sound broken and the RF signal is dirty.		
● Measurement instrument connections	Connect the oscilloscope to TP201, Pin 1 (RF). (Servo•digital board assy) [Settings] 20 mV/division 500 ns/division AC mode	● Player state ● Adjustment location ● Disc	Test mode, play VR105 (FE. OFS) YEDS-7

[Procedure]

1. Move the pickup to midway across the disc (R=35mm) with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys. Press the TRACK FWD ▷▷▯ key, the PLAY ▷ key, then the PAUSE ▯▯ key in that order to close the respective servos and put the player into play mode.
2. Adjust VR105 (FE. OFS) so that the 3T waveform at TP201, Pin 1 (RF) is maximum.



Out of adjustment



Optimum adjustment

13. Focus Servo Loop Gain Adjustment

Adjustment 2

● Objective	To optimize the focus servo loop gain.		
● Symptom when out of adjustment	Playback does not start or focus actuator noisy.		
● Measurement instrument connections	See Fig. 8 (Servo • digital board assy) [Settings] CH 1 : 0.1 V/division X-Y mode CH 2 :10 mV/division	● Player state ● Adjustment location ● Disc	Test mode, play VR201 (FCS. GAIN) (Servo • digital board assy) YEDS-7

[Procedure]

1. Set the AF generator output to 1.2kHz and 1Vp-p.
2. Move the pickup to midway across the disc (R=35mm) with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys. Press the TRACK FWD ▷▷▯ key, the PLAY ▷ key, then the PAUSE ▯▯ key in that order to close the respective servos and put the player into play mode.
3. Adjust VR201 (FCS. GAIN) so that the lissajous waveform is symmetrical about the X axis and the Y axis.

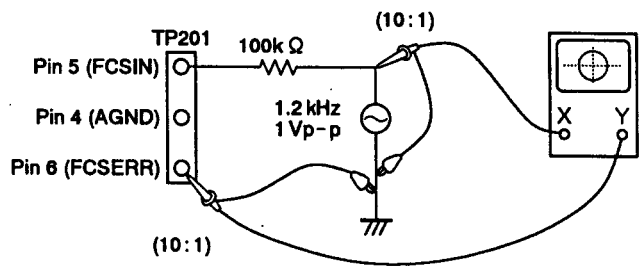
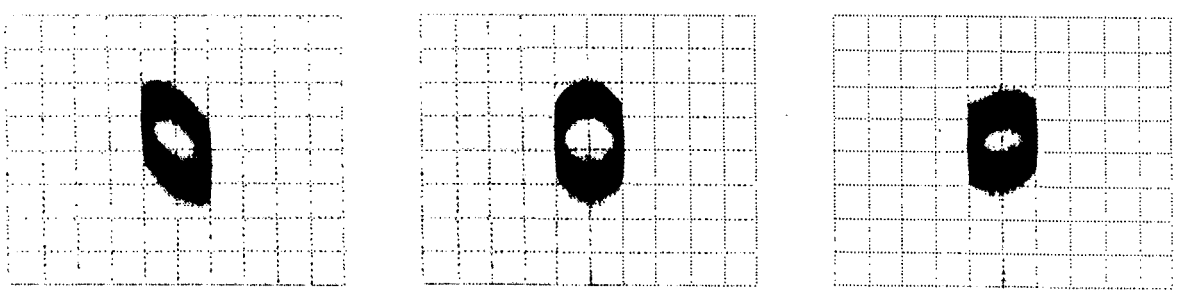


Fig. 8



Higher gain　　Optimum gain　　Lower gain

14. Tracking Servo Loop Gain Adjustment

Adjustment 2

● Objective	To optimize the tracking servo loop gain.		
● Symptom when out of adjustment	Playback does not start, during searches the actuator is noisy, or tracks are skipped.		
● Measurement instrument connections	See Fig. 9. (Servo • digital board assy) [Settings] CH 1 : 0.1 V/division X - Y mode CH 2 :10 mV/division	● Player state ● Adjustment location ● Disc	Test mode, play VR202 (TRK. GAIN) (Servo • digital board assy) YEDS - 7

[Procedure]

1. Set the AF generator output to 1.2kHz and 2Vp - p.
2. Move the pickup to midway across the disc (R=35mm) with the MANUAL SEARCH FWD ▷▷ or REV ◁◁ keys. Press the TRACK FWD ▷▷▯ key, the PLAY ▷ key, then the PAUSE ▯▯ key in that order to close the respective servos and put the player into play mode.
3. Adjust VR202 (TRK. GAIN) so that the lissajous waveform is symmetrical about the X axis and the Y axis.

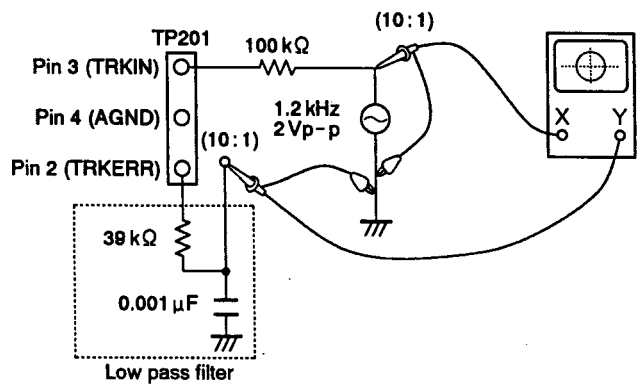
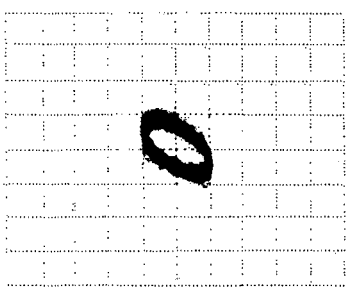
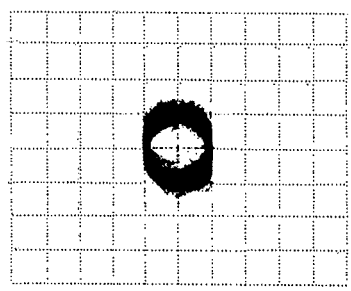


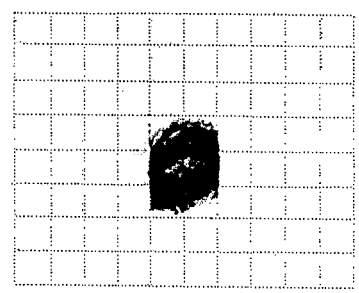
Fig. 9



Higher gain



Optimum gain



Lower gain

10. PARTS LIST FOR EXPLODED VIEWS AND PACKING

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

10.1 EXTERIOR SECTION

Mark	No.	Description	Part No.
	1	HEAD board assy	PWF1002
	2	SERVO•DIGITAL board assy	PWM1717
	3	AUDIO board assy	PWM1719
NSP	4	POWER SUPPLY board assy	PWZ2461
NSP	5	ST board assy	PWZ2891
	6	13P Flexible cable (30V)	PDD1144
	7	21P Flexible cable (30V)	PDD1145
	8	Earth lead unit (100L)	PDF1154
	9	AC cord plate	PNB1515
	10	Function switch (POWER)	PSG1011
	11	Ferrite core	PTH1018
⚠	12	Power transformer (servo)	PTT1292
⚠	13	Power transformer (audio)	PTT1293
	14	Wire assy	PXA1511
⚠	15	Fuse (2A)(FU10)	VEK1019
	16	Earth plate	PBK1090
	17	Hexagonal pole	PLA1128
NSP	18	Main chassis K	PNA2175
NSP	19	Side angle	PNB1151
NSP	20	PCB angle	PNB1253
NSP	21	Shield case	PNB1451
NSP	22	Case angle	PNB1452
NSP	23	Shield plate	PNB1453
NSP	24	Shield angle	PNB1454
NSP	25	Switch angle	PNB1455
	26	Sub plate	PNB1464
	27	Washer	PNM1127
	28	Rear panel KU	PNS1046
	29	Leg assy	PXA1524
	30	Leg assy	PXA1525
NSP	31	PCB angle A	RNB1083
	32	Screw	ABA1192
	33	Cushion B	DEB1197
NSP	34	Edge guard (B)	DEC1144
NSP	35	Cord holder	DNF1128
NSP	36	Absorption tape	PNM1128
	37	Rubber spacer (4.5)	PEB1258
	38	Rubber spacer	PEB1260
NSP	39	Wire clip	PEC-097
NSP	40	Edging H	PEC1014
NSP	41	Edging N	PEC1024
NSP	42	Absorption tape	PNM1172
NSP	43	Binder holder	PNW1021
NSP	44	P plate holder	PNY-405

Mark	No.	Description	Part No.
	45	Screw	BBZ40P080FCC
NSP	46	Rubber spacer	REB1118
	47	Cord clamper	RNH-184
NSP	48	PCB support	VEC1268
NSP	49	Tray assy	PXA1513
NSP	50	Single mechanism assy	PXA1516
	51	Side panel	AMR2319
	52	Power knob	PAC1650
	53	SH screw	PBA1049
	54	Side spacer	PEB1208
NSP	55	Earth lead unit	PDF1122
	56	Top plate R	PNS1027
	57	Side board	PNS1041
	58	Top plate F	PNS1042
	59	Ornamental screw	VBA1028
NSP	60	Absorption rubber (A)	VEB1084
	61	Tray panel	PAN1301
	62	Screw	PBA1024
	63	Spring	PBH1164
	64	Earth spring	PBH1165
	65	Absorption rubber A	PEB1264
	66	Absorption rubber B	PEB1265
NSP	67	Panel holder	PNW2318
NSP	68	Tray holder	PNW2319
	69	Washer	VBE1001
	70	Caution label	PRW1244
⚠	71	AC power cord	PDG1015
	72	Screw	BBT30P060FCC
	73	Screw	BBT30P080FCC
	74	Cord stopper	CM-22C
	75	Screw	IBZ30P060FCC
	76	Screw	IBZ30P080FCC
	77	Screw	PMF30P080FCU
	78	Screw	PMZ30P060FCC
	79	ICP caution label	PRW1383
	80	ICP caution label	PRW1384
	81	65 label	ORW1069
	82	Connector assy (2P)	PDE1252
NSP	83	MUTE board assy	PWX1386
	84	Washer	WH30FUC
	85	Washer	WH40FUC
	86	Screw	BBZ30P060FCC
	87	Screw	BBZ30P080FCC
	88	Flexible shield	PNM1232
	89	Absorption tape	PNM1045

10.2 FRONT SECTION

Mark	No.	Description	Part No.
NSP	1	H.P. board assy	PWZ2452
NSP	2	VOL. board assy	PWZ2454
NSP	3	FUNCTION board assy	PWZ2464
	4	22P flexible cable(30V)	PDD1156
	5	2mm pitch connector assy(7P)	PDE1231
	6	2mm pitch connector assy(9P)	PDE1237
	7	• • • • •	
	8	INPUT button	PAC1621
	9	Function button B	PAC1623
	10	Function button C	PAC1624
	11	Phones knob	PAC1745
	12	Function button A	PAC1747
	13	Pause button	PAC1748
	14	REC button (Gold)	PAC1764
	15	Function panel	PAM1555
	16	Display window	PAM1620
	17	FL sheet	PAM1663
	18	Front panel KU	PAN1300
	19	Door panel	PAN1295
	20	Screw	PBA1024
	21	SW spring	PBH1139
	22	Lock arm spring	PBH1140
NSP	23	Earth arm	PBK1102
NSP	24	Door earth	PBK1103
NSP	25	Lock spring	PBK1106
	26	• • • • •	
NSP	27	Door cushion	PED1013
NSP	28	Magnet	PMF1010
NSP	29	Back yoke D	PNB1390
NSP	30	Door yoke	PNB1391
	31	• • • • •	
	32	LED lens	PNW2019
	33	DISP lens	PNW2113
	34	REC lens	PNW2114
NSP	35	Door arm R	PNW2117
NSP	36	Lock arm	PNW2118
	37	Panel escutcheon	PNW2317
NSP	38	Door holder assy	PXT1048
	39	Door arm assy	PXT1058
	40	VR knob	RAA1018
	41	Name plate	RAN1011
	42	Damper assy	REC1013
	43	Indicator lens	PEA1206
	44	Sensor acrylic	VNK1566
	45	Screw	BBZ20P060FMC
	46	Screw	BMZ26P040FNI
	47	Screw	PBZ20P060FMC
	48	Door panel assy	PEA1303
	49	• • • • •	
	50	Screw	BBZ26P060FMC

10.3 SINGLE MECHANISM ASSY

Mark	No.	Description	Part No.
	1	Lever switch	DSK1003
	2	Float screw	PBA1079
	3	Bias spring	PBH1112
	4	Float spring (A)	PBH1167
	5	Float spring (B)	PBH1168
	6	Float spring (C)	PBH1169
	7	Float spring (D)	PBH1170
NSP	8	Connector assy (6P)	PDE1110
NSP	9	Connector assy (4P)	PDE1111
NSP	10	Earth lead unit	PDF1074
	11	Earth lead unit (150L)	PDF1153
	12	Earth lead unit (100L)	PDF1154
	13	Stopper rubber	PEB1085
	14	Belt	PEB1138
	15	Damper rubber	PEB1146
NSP	16	Rubber spacer	PEB1216
NSP	17	Rubber spacer	PEB1255
NSP	18	Absorption felt	PED-047
NSP	19	Sync. gear shaft	PLA1079
NSP	20	Gear angle	PNB1246
NSP	21	Bottom plate	PNB1258
NSP	22	Base plate	PNB1259
NSP	23	Mechanism deck	PNB1292
NSP	24	Mechanism cover	PNB1456
	25	Sub plate	PNB1464
	26	Gear	PNW1097
	27	Motor pulley	PNW1643
	28	Cam	PNW1816
	29	Sync. gear	PNW1817
	30	Gear pulley	PNW1870
	31	Single gear	PNW1878
NSP	32	U guide	PNW1880
	33	Roller	PNW2037
	34	Loading base L	PNW2050
	35	Loading base R	PNW2051
NSP	36	Collar	PNW2329
	37	DC motor /0.75W	PXM1010
	38	Door sheet	REB1191
	39	Cord clamper	RNH-184
NSP	40	Servo mechanism assy	PXA1490
	41	Screw	BBZ30P060FCC
	42	Screw	BBZ30P080FCC
	43	Screw	BMZ26P050FCU
	44	Screw	BPZ26P060FCU
	45	• • • • •	
	46	Screw	IPZ30P060FCU
	47	Screw	IPZ30P100FCU
	48	Screw	PDZ30P060FCC
	49	Screw	PMA26P040FCU
	50	Screw	PMZ26P040FCU

Mark	No.	Description	Part No.
	51	Washer	WT26D047D025
	52	Washer	WT31D054D013
	53	Washer	WT32D080D050
	54	TOC board assy	PWM1774
NSP	55	Plate magnet	DNS1052
	56	Skew spring	PBH1155
	57	Lock plate spring	PBH1156
	58	Shaft pressure spring	PBK1121
	59	Plate spring S	PBK1122
	60	Plate spring L	PBK1123
	61	TAN spring unit	PBK1124
	62	Guide shaft	PLA1120
	63	Roller	PLM1001
NSP	64	Side yoke	PNB1438
NSP	65	Center yoke	PNB1439
	66	Slit plate	PNM1212
	67	Carriage unit	PNR1060
	68	Mechanism chassis	PNW2254
	69	• • • • •	
	70	• • • • •	
	71	Lock plate	PNW2257
	72	Spindle motor	PXM1036
	73	Disc table assy	PXT1050
	74	Rivet	DEC1318
	75	Screw	PBA1024
	76	Adjusting screw (L=10)	PBA1076
	77	Adjusting screw (L=12)	PBA1077
	78	• • • • •	
	79	Stopper rubber	PEB1035
	80	Screw C	VBA1014
	81	Pickup assy	PEA1283
	82	Screw	BBZ26P060FMC
	83	Screw	BBZ26P080FCC
	84	Screw	BMZ20P030FNI
	85	Screw	BMZ26P060FMC
	86	Screw	IPZ20P050FMC
	87	Screw	JGZ20P035FZK
	88	Screw	PMF20P050FMC
	89	Screw	PMH20P040FMC
	90	Washer	WT26D047D025
	91	Screw	ZMD26H040FBT
	92	Drive coil assy	PEA1304
	93	Speed detection coil assy	PEA1305
	94	Drive yoke assy	PEA1306
	95	Speed detection yoke assy	PEA1307

10.4 TRAY ASSY

Mark	No.	Description	Part No.
	1	Turn table	PAN1203
	2	Float screw	PBA1064
	3	Float spring	PBH1092
NSP	4	Earth lead unit	PDF1074
	5	Damper rubber	PEB1146
NSP	6	Stopper rubber	PEB1148
NSP	7	Absorption felt	PED-047
NSP	8	Tray	PNA2027
NSP	9	Thrust holder	PNB1294
	10	TT Absorption sheet	PNM1125
	11	Double sided adhesive tape	PNM1129
NSP	12	Absorption tape	PNM1132
NSP	13	Collar	PNW2012
NSP	14	Tray locker	PNW2014
	15	Over tray	PNW2079
NSP	16	Slide guide	PNW2080
NSP	17	Rack	PNW2081
	18	Spindle base assy	PXA1405
	19	Rotor assy	PXA1515
	20	Thrust ball catch	VNL-268
	21	Screw	BBZ30P060FCC
	22	Screw	IBZ30P060FCC
	23	Screw	IPZ30P060FCU
	24	E ring	YE30FUC
	25	Turn table assy	PEA1294

10.5 PACKING

Mark	No.	Description	Part No.
	1	Cord with mini plug	PDE1247
	2	Turn table sheet assy	PEA1174
NSP	3	Rubber spacer	PEB1174
	4	Protector sheet	PHC1076
	5	Spacer	PNM1229
	6	Operating instructions (English)	PRB1221
	7	Caution card	PRM1028
	8	Sheet	PRW1245
	9	Remote control unit (CU-PD057)	PWW1071
	10	Battery cover	PZN1009
	11	Connection cord assy	RDE1013
NSP	12	Battery (R03,AAA)	VEM-022
	13	Polyethylene bag	Z21-038
	14	Transportation screw	PBA1078
	15	Protector F	PHA1246
	16	Protector R	PHA1247
	17	Packing case	PHG2089
	18	Mirror mat	VHL1012
	19	Top plate	PHC1047
	20	CD-R disc caution card	PRM1031
	21	Polyethylene bag	Z21-013

11. PCB PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex.1 When there are 2 effective digits(any digit apart from 0), such as 560 ohm and 47k ohm(tolerance is shown by J=5%, and K=10%).

560Ω → 56 × 10¹ → 561 ..... RD1/8PM 5 6 1 J
47kΩ → 47 × 10³ → 473 ..... RD1/4PS 4 7 3 J
0.5Ω → 0R5 ..... RN2H 0 R 5 K
1Ω → 010 ..... RS1P 0 1 0 K

Ex.2 When there are 3 effective digits(such as in high precision metal film resistors).

5.62kΩ → 562 × 10¹ → 5621 ..... RN1/4PC 5 6 2 1 F

Mark	No.	Description	Part No.
LIST OF ASSEMBLIES			
		HEAD BOARD ASSY	PWF1002
		SERVO•DIGITAL BOARD ASSY	PWM1717
		AUDIO BOARD ASSY	PWM1719
NSP		MUTE BOARD ASSY	PWX1386
		POWER BOARD ASSY	PWR1025
NSP		├POWER SUPPLY BOARD ASSY	PWZ2461
NSP		└ST BOARD ASSY	PWZ2891
		FRONT BOARD ASSY	PWX1256
NSP		├H. P. BOARD ASSY	PWZ2452
NSP		├VOL. BOARD ASSY	PWZ2454
NSP		└FUNCTION BOARD ASSY	PWZ2464
NSP		SINGLE MECHANISM ASSY	PXA1516
NSP		└SERVO MECHANISM ASSY	PXA1490
		└TOC BOARD ASSY	PWM1774
HEAD BOARD ASSY			
SEMICONDUCTORS			
		IC102	CXD7500M
⚠		IC106	LA6517
⚠		IC108	LB1687
		IC104	NJM4560M
		IC101	PA4020A
⚠		IC109	TA8410AK
		IC103	TC74HC00AF
		IC105	TC74HC08AF
		IC107	UPC812C
		Q102-Q108, Q110	2SA1461
		Q101	2SC2412K
		Q109	DTC124ES
		D101	1SS133X
		D102, D103	DAN202K
COIL AND FILTERS			
		F31-F33, F35	DTF1064
		L30	LFA100K
		F36	DTF1067
CAPACITORS			
		C140	CCSQCH020D50
		C186	CCSQCH050D50
		C145	CCSQCH100D50
		C103, C142	CCSQCH100J50
		C172	CCSQCH101J50
		C128	CCSQCH181J50
		C133	CCSQCH220J50
		C123, C124, C136	CCSQCH221J50
		C109-C112	CCSQCH391J50
		C122	CCSQCH620J50
		C105-C108	CCSQSL821J50
		C175	CEANP100M16
		C117, C127	CEANP2R2M25
		C116	CEAS100M16
		C144	CEAS100M50
		C101, C102, C113, C119, C121	CEAS101M10
		C125, C129, C134, C151, C153	CEAS101M10
		C156, C158, C165, C167	CEAS101M10
		C170, C180	CEAS330M25
		C160	CFTXA474J50
		C114, C130, C131, C137, C138	CKSQYB103K50
		C141, C174, C176, C182-C184	CKSQYB103K50
		C115, C132, C173	CKSQYB104K25
		C162, C163	CKSQYB333K25
		C150, C155, C161, C177-C179	CKSQYB473K25
		C104, C118, C120, C126, C135	CKSQYF103Z50
		C139, C152, C154, C157, C159	CKSQYF103Z50
		C164, C166, C168, C171, C181	CKSQYF103Z50
		C143	CKSQYF104Z50
RESISTORS			
		R148(2.2kΩ)	DCN1028
		R129, R130(120Ω)	PCN1027
⚠		R173	RS1LMFR47J
		VR101, VR103-VR108, VR112(10kΩ)	RCP1045
		VR102, VR110, VR111(22kΩ)	RCP1046
		Other Resistors	RS1/10S□□□J
OTHERS			
		CN105 MT CONNECTOR 3P	173981-3
		CN101 FLEXIBLE CONNECTOR	5597-26APB
		CN102 FFC CONNECTOR 13P	HLEM13R-1
		CN106 FFC CONNECTOR 21P	HLEM21R-1
		EARTH METAL	VNF-091

SERVO•DIGITAL BOARD ASSY

SEMICONDUCTORS

Mark	No.	Description	Part No.
	IC201		CXA1372Q
	IC225		CXD2500BQ
	IC222		G307PA23
	IC318	(HM6264ALFP-12T)	GGF9002
⚠	IC231		LA6517
	IC311		LC89583
	IC227		LH5116-15
	IC206		M5238AP
	IC301		M65810FP
	IC315		M65811FP
	IC306	(MB814800A-80PZ)	GGC1057
	IC308, IC310		MC74HC4046AN
	IC207, IC209, IC224		NJM2903D
	IC215, IC223		NJM2904D
	IC213, IC214		NJM311D
	IC203, IC208, IC210, IC211, IC216		NJM4560D
	IC219-IC221		NJM4560D
⚠	IC236		NJM78L05A
	IC316		PCX1021
	IC309		PD0026A
	IC320		PD2020
	IC304		PD4469A
	IC307		PD6093A
	IC305		PD6107A
	IC226		PD6118C
	IC312		SM5813AP
	IC313, IC323		TC74HC04AP
	IC233		TC74HC138AP
	IC314, IC322		TC74HC153AP
	IC230, IC303		TC74HC367AP
	IC202		TC74HC4051AP
	IC204, IC217		TC74HC4053AP
	IC205, IC232		TC74HC4094AP
	IC229		TC74HC573AP
	IC234		TC74HC574AP
	IC302, IC317		TC74HCU04AP
	IC235		TC7S00F
	IC319		TC7S08F
	IC218		TC7S32F
	IC321		TC9231N
	IC228	(UPD78323GJ-5BJ)	GGC1056
	Q206, Q207, Q209, Q210		2SA933S
	Q204, Q205, Q211-Q213, Q311		2SC1740S
	Q308		2SC1740SLN
	Q304, Q309, Q310		DTA114ES
	Q305, Q306		DTA114TS
	Q202, Q214		DTA124ES
	Q303		DTC114ES
	Q302, Q307		DTC114TS
	Q201, Q203, Q208		DTC124ES
	Q301		DTC144ES
	D201-D216, D220, D301		1SS133X
	D303-D306		1SS133X

COILS AND FILTERS

Mark	No.	Description	Part No.
	F301-F309, F311, F312		DTF1067
	F320-F324		DTF1067
	L203-L205		LFA100K
	L328		PTF1016
	L313		PTL1003
	L201, L202, L206, L301		RTF1163
	L304-L308, L311, L315-L323		RTF1163
	L302, L303, L312, L325		VTH1020
	L340		LAU1R2J

SWITCHES

S301, S302		RSH1025

CAPACITORS

C1324	CCCCH101J50
C1312, C1314, C315, C353, C375	CCSQCH100D50
C999	CCSQCH100D50
C1302-C1304, C1313, C1316, C1319	CCSQCH101J50
C283, C387, C399, C962	CCSQCH101J50
C906, C907	CCSQCH150J50
C251, C252	CCSQCH151J50
C343	CCSQCH181J50
C330	CCSQCH220J50
C277, C278, C281, C282	CCSQCH331J50
C230, C231, C354-C356	CCSQCH470J50
C1318	CCSQCH471J50
C310, C318, C319	CCSQCH560J50
C364	CCSQCH820J50
C325	CCSQSL101J50
C206, C244, C260, C261, C289	CEAS010M50
C272, C288	CEAS0R1M50
C922	CEAS100M50
C210, C212, C222, C223	CEAS101M10
C242, C243, C245-C247	CEAS101M10
C1330, C1331	CEAS100M16
C262, C263, C268-C270	CEAS101M10
C274, C275, C279, C280, C287	CEAS101M10
C290, C302, C309, C312, C321	CEAS101M10
C323, C329, C333, C335, C341	CEAS101M10
C345, C349, C358, C360, C361	CEAS101M10
C369, C374, C376, C382, C384	CEAS101M10
C902, C909, C911, C912	CEAS101M10
C273, C284	CEAS2R2M50
C219, C221, C226, C228, C229	CEAS470M10
C236, C237, C257, C259	CEAS470M10
C337	CEAS470M16
C921	CEAS470M50
C295	CEAS471M6R3
C203, C234, C235	CEAS4R7M50
C294	CEASR47M50
C314	CFTXA102J50
C379	CFTXA103J50
C306, C307, C311, C344, C363	CFTXA104J50
C317, C378	CFTXA105J50
C316	CFTXA224J50
C1311	CGCYF104Z25
C1321, C970-C973	CKCYF103Z50
C1325, C241, C324, C331, C1325	CKSQYB102K50
C207, C211, C216, C224, C293	CKSQYB103K50
C304, C338, C351, C913-C918	CKSQYB103K50

Mark	No.	Description	Part No.
	C201, C202, C204, C205, C240		CKSQYB104K25
	C254, C264, C265		CKSQYB104K25
	C292		CKSQYB152K50
	C271		CKSQYB272K50
	C285		CKSQYB273K50
	C217		CKSQYB332K50
	C209, C215, C253, C926		CKSQYB333K25
	C276, C995		CKSQYB471K50
	C213, C214, C233, C250		CKSQYB472K50
	C298		CKSQYB473K25
	C286		CKSQYB681K50
	C297		CKSQYB683K25
	C336		CKSQYF102Z50
	C1301, C1315, C208, C218, C220		CKSQYF103Z50
	C225, C227, C232, C238, C239		CKSQYF103Z50
	C255, C256, C258, C266, C267		CKSQYF103Z50
	C301, C305, C308, C313, C320		CKSQYF103Z50
	C322, C326, C328, C334		CKSQYF103Z50
	C340, C342, C346-C348, C350		CKSQYF103Z50
	C357, C359, C362, C365-C368		CKSQYF103Z50
	C370, C372, C373, C377		CKSQYF103Z50
	C380, C381, C383, C901		CKSQYF103Z50
	C903-C905, C908, C910		CKSQYF103Z50
	C923, C924, C963		CKSQYF103Z50
	C296, C303, C332, C339, C396, C398, C960		CKSQYF104Z25
	C965, C966, C1326		CKSQYF104Z25
	C248, C249, C291, C327		CKSQYF473Z25
	C919, C920, C925		CKSQYF473Z25
	C299		CKSYF224Z25
RESISTORS			
	R989(24kΩ/48kΩ)		PCN1033
	R981-R984		RS1/10S244F
	R1370, R1371		RD1/6PM123J
	VR201, VR202(10kΩ)		RCP1045
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN202 MT CONNECTOR 4P		173981-4
	CN203 MT CONNECTOR 6P		173981-6
	CN208 5P TOP POST		B5P-SHF-1AA
	CN204 KR CONNECTOR		B6B-PH-K
	CN207, CN209 6P TOP POST		B6P-SHF-1AA
	CN201 FFC CONNECTOR 21P		HLEM21S-1
	CN206 FFC CONNECTOR 22P		HLEM22S-1
	EARTH PLATE(TINPLATE)		PBK1130
	J305 CONNECTOR ASSY(3P)		PDE1253
	J304 CONNECTOR ASSY(4P)		PDE1254
⚠	LITHIUM BATTERY		PEM1003
	JA306, JA307 REMOTE CONTROL JACK/12V		PKN1004
	X201 CERAMIC RESONATOR(16MHz)		PSS1010
	JA303, JA305 1P PIN JACK		RKB1012
	JA301, JA302 OPTICAL RECEIVE MODULE		TORX178A
	JA304 OPTICAL TRANSMISSION MODULE		TOTX178
	PCB BINDER		VEF1008
	EARTH METAL		VNF-091
	X301 CERAMIC RESONATOR(4.19MHz)		VSS1014

Mark	No.	Description	Part No.
AUDIO BOARD ASSY			
SEMICONDUCTORS			
	IC804		CS5339
⚠	IC413, IC414, IC601-IC604		ICP-N10
	IC405, IC406, IC409, IC410		NJM2114D
	IC801, IC802		NJM2114D
⚠	IC403, IC411, IC412		NJM78M05FA
⚠	IC401		NJM78M15FA
⚠	IC404		NJM79M05FA
⚠	IC402		NJM79M15FA
	IC407, IC408		PD2029A
	IC419		TC74HC00AF
	IC417		TC74HCU04AF
	IC803, IC807		UPC812C
⚠	Q402		2SB942
	Q411, Q412, Q417-Q420		2SC3068
⚠	Q401		2SD1267
⚠	Q415, Q416		2SJ104
⚠	Q413, Q414		2SK364
	Q403, Q404, Q406-Q408		DTA124ES
	Q405, Q409, Q410		DTC124ES
	Q422		2SA933LN
	Q421		2SC1740LN
⚠	D401-D412		10DF2
	D415-D419, D801-D804		1SS254
⚠	D413, D414		HZ6B1L
COILS			
	L424		PTF1016
	L419-L421, L423, L425		PTH1013
	L428-L431, L433, L455, L456, L801		PTH1013
	L806, L807, L815		PTH1013
	L808, L809		PTH1014
	L409-L411, L416-L418, L427		PTH1016
	L436-L440, L450-L454, L802-L805		PTH1016
	L810-L814, L816		PTH1016
	L434, L435, L441		PTH1017
	L408, L412-L415		VTH1020
CAPACITORS			
	C499, C500, C514, C517, C527		CCCCH100D50
	C835, C836		CCCCH100D50
	C515, C525, C529, C530, C536		CCCCH101J50
	C487		CCCCH120J50
	C524		CCCCH121J50
	C488		CCCCH270J50
	C455-C462		CCCCH390J50
	C526		CCCCH680J50
	C411, C412		CENA010M50
	C413-C416		CENA100M50
	C486		CENA101M10
	C809, C810		CENA101M25
	C805-C808, C811, C812		CENA221M25
	C431		CENA470M50
	C433, C434, C437, C438		CENA471M16
	C449-C452, C823, C825, C828		CENA471M16
	C469-C472		CENA471M25
	C419, C420		CENA471M50
	C424, C425		CENA472M16
	C818		CEYA100M50

Mark	No.	Description	Part No.
	C803, C804		CEYANP220M50
	C813, C814		CEYANP330M25
	C426-C430, C432, C439-C442		CFTXA103J50
	C453, C454, C485, C489-C492		CFTXA103J50
	C528, C815, C816		CFTXA103J50
	C435, C436, C445-C448, C480		CFTXA104J50
	C483, C543, C819, C822, C824		CFTXA104J50
	C826, C827, C830, C831		CFTXA104J50
	C820, C821		CFTXA105J50
	C477, C478		CFTXA152J50
	C443, C444		CFTXA473J50
	C465, C466		CFTXA562J50
	C409, C410, C417, C418		CFTXA563J50
	C467, C468		CFTXA681J50
	C463, C464		CFTXA683J50
	C520		CKCYB102K50
	C523		CKCYB182K50
	C522		CKCYB222K50
	C496		CKCYB471K50
	C493		CKCYB472K50
	C401-C406, C421-C423, C484		CKCYF103Z50
	C521, C531		CKCYF103Z50
	C817		CQPA103J100
	C473, C474 (47 μ, AC50V)		PCH1094
	C475, C476 (220 μ, AC35V)		PCH1099
	C407 (3300 μ, 50V)		RCH1046
	C408 (3300 μ, 50V)		RCH1047
RESISTORS			
	R821		RDR1/4PM101J
	R424, R425, R483, R488		RDR1/4PM102J
	R404, R405		RDR1/4PM103J
	R803, R804, R807, R808		RDR1/4PM104J
	R452, R453		RDR1/4PM105J
	R813, R814		RDR1/4PM152J
	R448, R449, R458, R459		RDR1/4PM162J
	R450, R451, R470, R471		RDR1/4PM221J
	R454, R455		RDR1/4PM222J
	R426-R433, R462, R463		RDR1/4PM223J
	R815, R816		RDR1/4PM240J
	R811, R812		RDR1/4PM270J
	R468, R469		RDR1/4PM271J
	R401-R403		RDR1/4PM474J
	R460, R461		RDR1/4PM331J
	R456, R457		RDR1/4PM332J
	R805, R806		RDR1/4PM333J
	R442-R445		RDR1/4PM433J
	R464, R465, R475		RDR1/4PM471J
	R408, R409, R809, R810		RDR1/4PM472J
	R801, R802		RDR1/4PM474J
	R486, R487		RDR1/4PM4R7J
	R817-R819		RDR1/4PM510J
	R466, R467, R472, R473		RDR1/4PM511J
	R406, R407		RDR1/4PM512J
	R446, R447		RDR1/4PM751J
	R434-R441		RDR1/4PM753J
	R411		RS1LMF222J
	R422, R423		RS1LMF562J
	Other Resistors		RD1/6PM□□□J

Mark	No.	Description	Part No.
OTHERS			
	CN403 3P TOP POST(VH)		B3P-VH
	SCREW		BBZ30P080FCC
	SCREW		IBZ30P100FCC
	EARTH PLATE(TINPLATE)		PBK1130
	LEAD WIRE UNIT		PDF1156
	X401 CRYSTAL RESONATOR(16.9344MHz)		PSS1008
	JA401, JA802 1P PIN JACK(W)		RKB1010
	JA402, JA801 1P PIN JACK(R)		RKB1011
	PCB BINDER		VEF1008
	EARTH METAL		VNF-091
	BINDER		Z09-056

MUTE BOARD ASSY

SEMICONDUCTORS

	Q8001, Q8002		2SD2114K
	Q8004		DTA124EK
	Q8003		DTC124EK
	D8001		DAP202K

RESISTORS

	Other Resistors		RS1/10S□□□J

POWER SUPPLY BOARD ASSY

SEMICONDUCTORS

⚠	IC16, IC17, IC7		ICP-N10
⚠	IC6		ICP-N15
⚠	IC1, IC14, IC15, IC2		ICP-N20
	IC10		M51957AL
⚠	IC5		NJM2114D
⚠	IC11-IC13		NJM7805FA
⚠	IC3, IC8		NJM7809FA
⚠	IC4, IC9		NJM7909FA
⚠	Q5		2SA1283
⚠	Q2		2SB942
⚠	Q1		2SD1267
	Q6		DTA144ES
⚠	D10, D12-D14		11DF2
⚠	D7		1SR35-100A
	D11		1SS254
⚠	D1-D4		31DF2-FC5
⚠	D5, D6		HZ3BLL
⚠	D8		MTZJ27A
	D9		MTZJ7.5A

COILS

⚠	L2		PTL1002
⚠	L1		PTL1009

SWITCH

⚠	S1		PSA1004

CAPACITORS

	C34		CEAS010M50
	C26, C28		CEAS101M50
	C27		CEAS470M35
	C12, C13		CENA010M50
	C16, C17, C31, C33		CENA102M16

Mark	No.	Description	Part No.
	C32		CENA221M50
	C14, C15		CENA330M25
	C22, C23		CENA471M50
	C35-C37		CFTXA105J50
	C10, C11, C18, C19		CFTXA473J50
	C24, C25, C30		CFTXA473J50
	C38-C45, C5-C7		CKCYF103Z50
	C29, C8, C9 (6800 μ, 25V)		RCH1016
⚠	C1 (0.01 μ, AC 400V)		VCG-044
RESISTORS			
	R9		RD1/2PMF152J
	R3, R6		RDR1/4PM103J
	R13-R16		RDR1/4PM304J
	R10		RDR1/4PM392J
	R1, R5		RDR1/4PM432J
	R2, R4		RDR1/4PM622J
	Other Resistors		RD1/6PM□□□J
OTHERS			
	CN3	3P TOP POST (VH)	B3P-VH
	CN4	5P VH CONNECTOR	B5P-VH
	J1	2MM PITCH CONNECTOR ASSY 11P	PDE1258
	J2	2MM PITCH CONNECTOR ASSY 9P	PDE1233
	HEAT SINK (AL)		PNS1043
⚠	TERMINAL		RKC-061
	PCB BINDER		VEF1008
	EARTH METAL		VNF-091

ST BOARD ASSY

COIL

L1380		LFA220K

SWITCH

S303		RSH1022

CAPACITORS

C1385, C1387, C1390		CCCCH101J50
C1380, C1383, C1388		CEAS101M10
C1381, C1382, C1384, C1389, C1391		CGCYF104Z25

OTHERS

JA311	OPTICAL TRANSMISSIN MODULE	1261AAC
JA310	OPTICAL RECEIVE MODULE	1361AAC
CN311	CONNECTOR 2P	53014-0210
CN312	KR CONNECTOR 3P	B3B-PH-K
CN310	KR CONNECTOR 4P	B4B-PH-K
EARTH METAL		VNF-091

Mark	No.	Description	Part No.

FUNCTION BOARD ASSY

SEMICONDUCTORS

IC702		M51957AL
IC703		MB88306P
IC701		PD4468D
Q701-Q705		2SC1740S
D707-D710, D712-D715		1SS254
D702		LD-701VR
D701		MTZ9.1B
D711		SEL2210S
D703-D706, D716		SLH-34VC35H3

COIL

L701		PTH1016

SWITCHES

S705		PSG1009
S701-S704, S706-S729		RSG1030

CAPACITORS

C703		CEJA220M50
C702		CEJA220M6R3
C705		CEJA2R2M50
C704, C708		CEJA470M16
C707, C709		CKCYF223Z50
C710-C735		CKPUYB121K50
C701, C706		CKPUYF223Z25

RESISTORS

R725		PCN1029
R703		PCN1030
R718		PCN1031
R701, R702		PCN1032
R719		RA4T222J
Other Resistors		RD1/6PM□□□J

OTHERS

CN702	CONNECTOR 2P	53025-0210
REMOTE SENSOR		GP1U58X
CN701	FFC CONNECTOR 22P	HLEM22R-1
V701	FL INDICATOR TUBE	PEL1071
X701	CERAMIC RESONATOR (4.19MHz)	VSS1014

H. P. BOARD ASSY

SEMICONDUCTORS

IC501		M5216L
Q501, Q502		2SC3068
D501, D502		1SS254

COILS AND FILTERS

L401-L406		VTH1020

CAPACITORS

C505-C507		CCCCH100D50
C508, C510, C512		CCCCH101J50
C503, C504		CENA470M25
C501, C502		CEYANP100M25
C509, C511, C513		CGCYF104Z25

RESISTORS

VR501 (20kΩ)		PCS1001
Other Resistors		RD1/6PM□□□J

Mark	No.	Description	Part No.
OTHERS			
	JA501	HEADPHONE JACK	RKN1001
	PCB BINDER		VEF1008

VOL. BOARD ASSY

SEMICONDUCTORS			
	IC805, IC806		M5238AP
CAPACITORS			
	C834, C835		CENA221M25
	C832, C833		CFTXA471J50
RESISTORS			
	R825, R826		RDR1/4PM104J
	R829, R830		RDR1/4PM472J
	R827, R828		RDR1/4PM561J
	VR802(20kΩ)		PCS1012
	VR801(20kΩ)		PCS1013
OTHERS			
	CN803	KR CONNECTOR 9P	S9B-PH-K

TOC BOARD ASSY

RESISTORS			
	Other Resistors		RD1/6PM□□□J
OTHERS			
	PHOTO INTERRUPTER		GP1A51HR
	LEAD WIRE UNIT		PDF1156
	BINDER		Z09-056

PIONEER®
The Art of Entertainment

Service Manual

ORDER NO.
RRZ1172

The chapter 1 of this Service Manual will not be reprinted. On your additional orders, we may supply only the chapter 2. For the chapter 1, please make copies and attach to the chapter 2 at your side if necessary.

COMPACT DISC RECORDER

PDR-09

CHAPTER 2

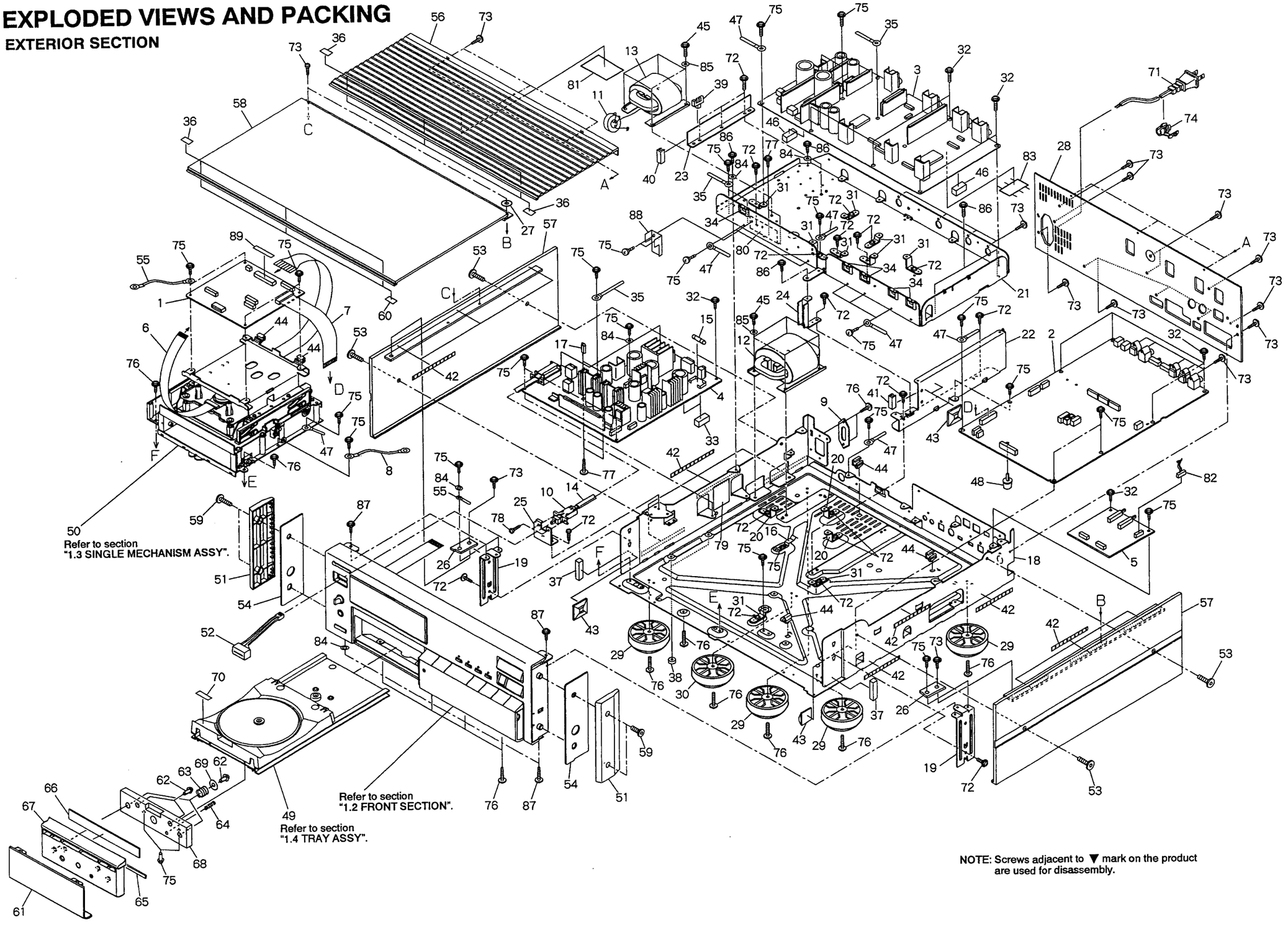
CONTENTS

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 300 Allstate Parkway Markham, Ontario L3R 0P2 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Haven 1087 Keetberglaan 1, 9120 Melsele, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

T-IFI JULY 1994 Printed in Japan

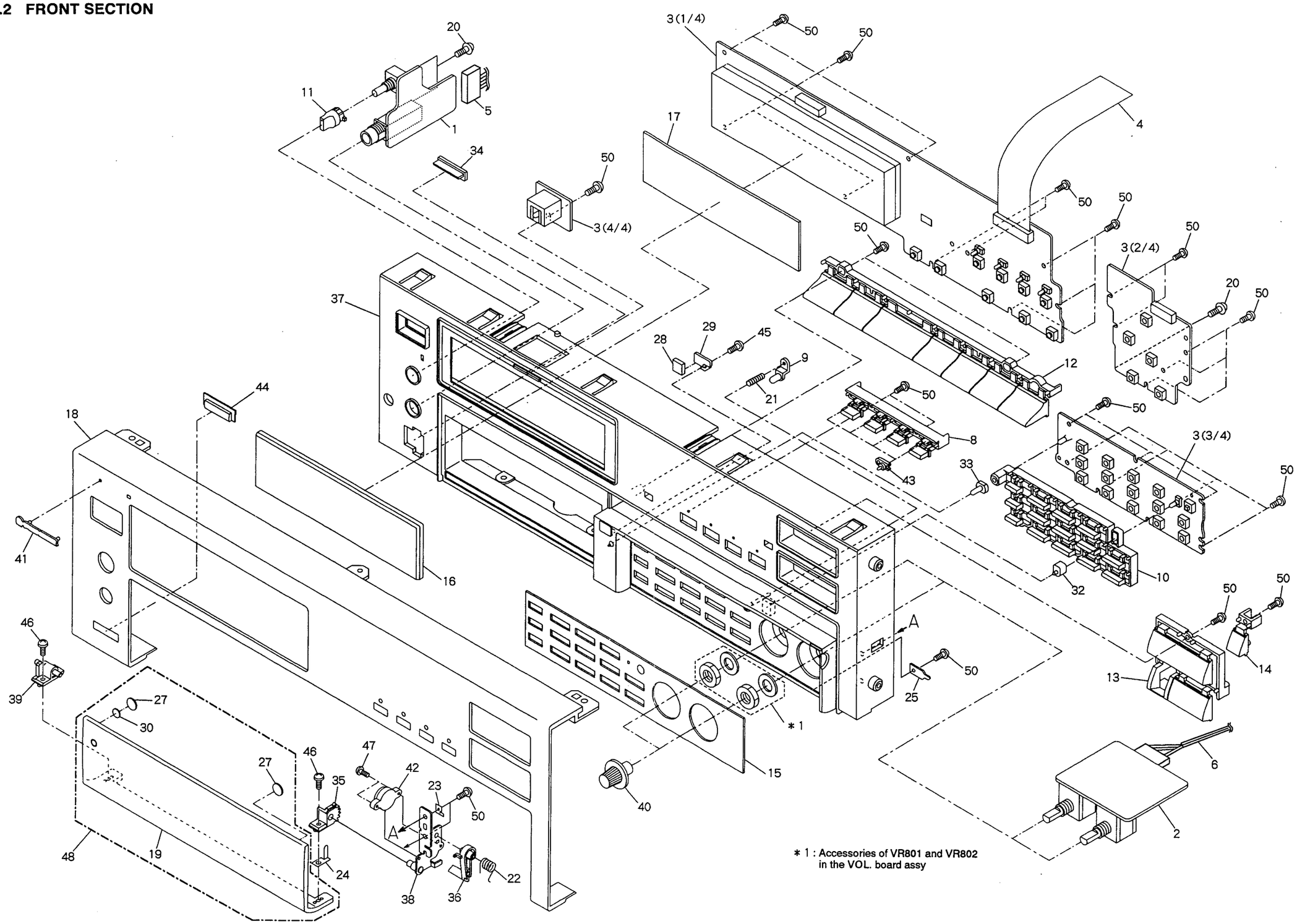
1. EXPLODED VIEWS AND PACKING

1.1 EXTERIOR SECTION



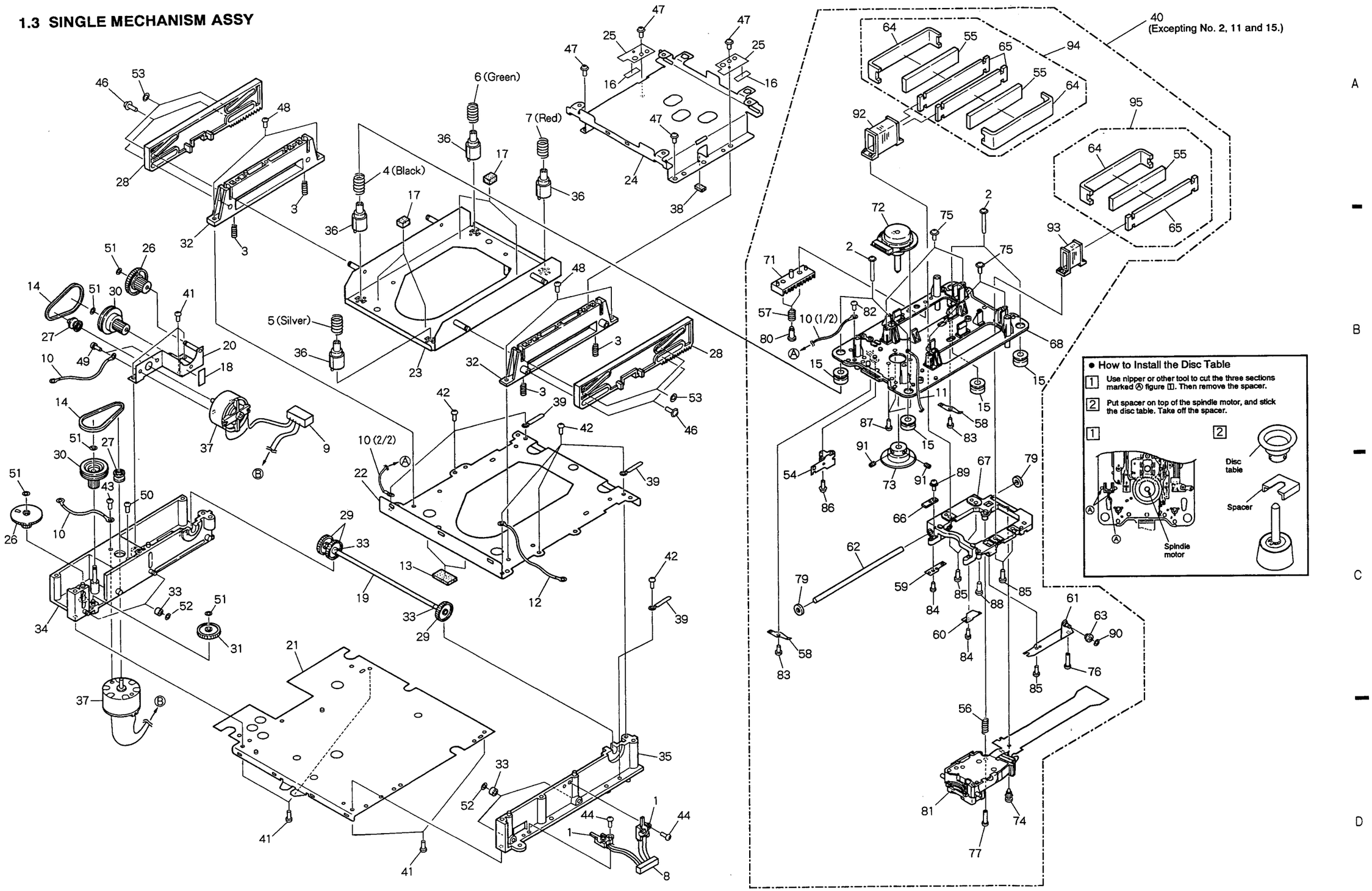
NOTE: Screws adjacent to ▼ mark on the product are used for disassembly.

1.2 FRONT SECTION

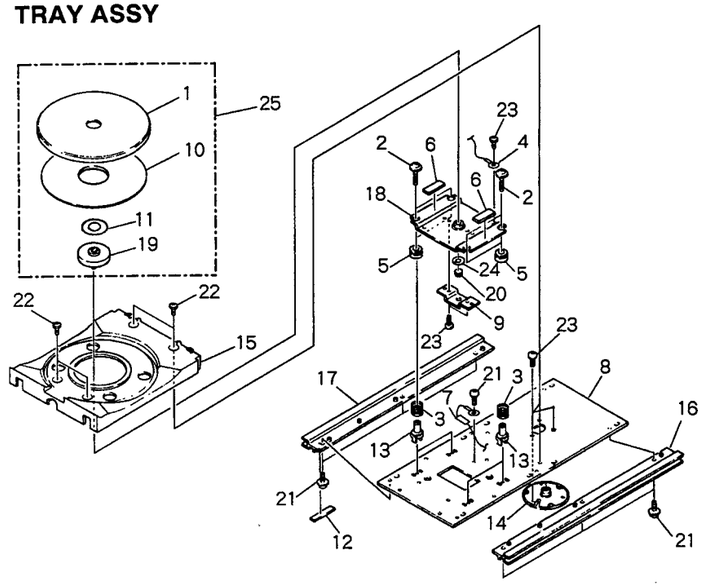


*1 : Accessories of VR801 and VR802 in the VOL. board assy

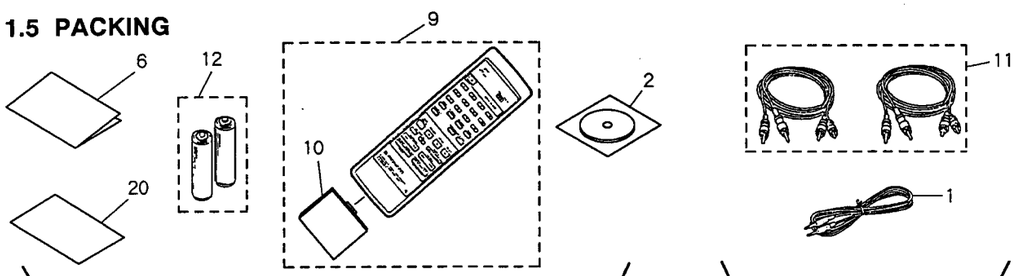
1.3 SINGLE MECHANISM ASSY

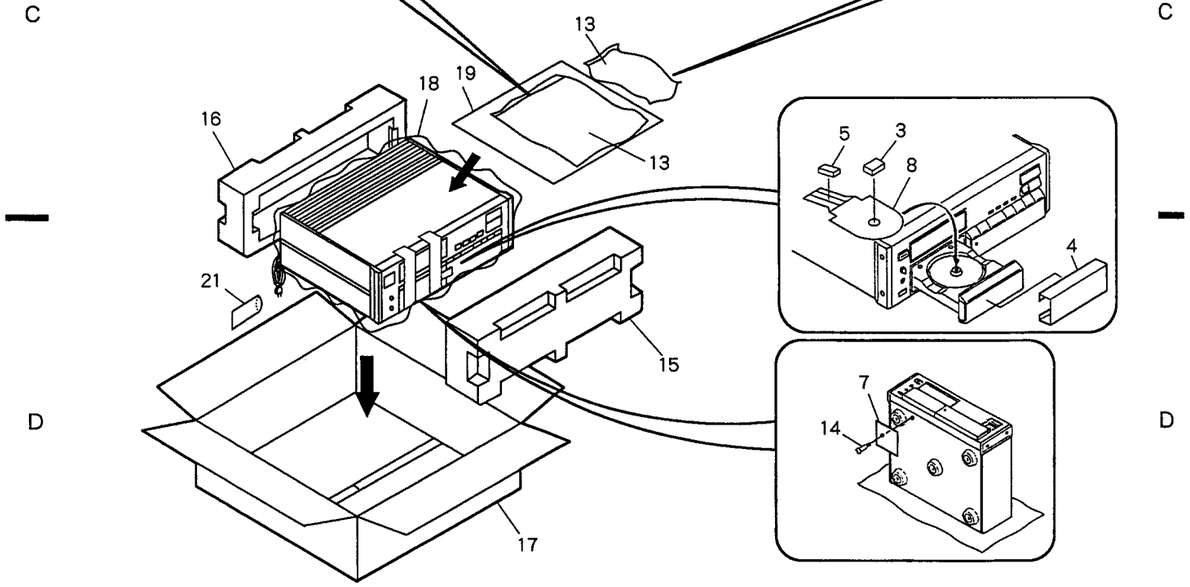


1.4 TRAY ASSY



1.5 PACKING





2. SCHEMATIC AND PCB CONNECTION DIAGRAMS

NOTE FOR SCHEMATIC DIAGRAMS (Type 4A)

1. **When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".**
2. **Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.**
3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance:(F):±1%, (G):±2%, (K):±10%, (M):±20% or ±5% unless otherwise noted.
4. **CAPACITORS:**
   Unit : p:pF or μF unless otherwise noted.
   Ratings : capacitor (μF) / voltage (V) unless otherwise noted.
   Rated voltage : 50V except for electrolytic capacitors.
5. **COILS:**
   Unit : m:mH or μH unless otherwise noted.
6. **VOLTAGE AND CURRENT:**
   ▭ or ←V :
   DC voltage (V) in PLAY mode unless otherwise noted.
   ⇦mA or ←mA :
   DC current in PLAY mode unless otherwise noted.
   Value in ( ) is DC current in STOP mode.
7. **OTHERS:**
   - ⊘ or ⊘ : Adjusting point.
   - ◀ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.
8. **SCH – □ ON THE SCHEMATIC DIAGRAM:**
   - SCH– □ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram.)
9. **SWITCHES** (Underline indicates switch position):
   OUT OF P.C.BOARD ASSEMBLY
   S101: OPEN/CLOSE
   S102: CLAMP/UP
   SERVO-DIGITAL BOARD ASSY
   S301: DIGITAL OUT ON – OFF
   S302: CD/CD-R SW
   FUNCTION BOARD ASSY
   S701: DISPLAY OFF
   S702: SKIP CLEAR
   S703: AREA SKIP
   S704: TRACK SKIP
   S705: SKIP ON – OFF
   S706: PEAK DISPLAY
   S707: AUTO REC/PAUSE
   S708: AUTO TRACK NO.
   S709: MANUAL TRACK NO.
   S710: INDEX NO.
   S711: PEAK RESET
   S712: TIME
   S713: PREVIOUS
   S714: FADE
   S715: TOC WRITE
   S716: OPTICAL 1
   S717: OPTICAL 2
   S718: COAXIAL
   S719: ANALOG
   S720: OPEN/CLOSE (▲)
   S721: STOP (■)
   S722: PLAY (▶)
   S723: TRACK (|◀◀)
   S724: TRACK (▶▶|)
   S725: REC (●)
   S726: PAUSE (||)
   S727: MANUAL (▶▶)
   S728: MANUAL (◀◀)
   S729: REC MUTE (■)
   POWER SUPPLY BOARD ASSY
   S1: POWER

NOTE FOR PCB DIAGRAMS:

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator

PION-04343 / DRUCK 6

1 2 3 4

LL WIRING DIAGRAM

POWER SUPPLY BOARD ASSY
(PWZ2461)
(➡ SCH – 7)

POWER CORD
DG1015

CN6
1 NEUTRAL
2 LIVE

CN2 / CN1
SWD100 / 100V

POWER TRANSFORMER
(SERVO)
PTT1292

POWER TRANSFORMER
(AUDIO)
PTT1293

B3P-VH CN3
1 +A17V
2 AUGND
3 −A17−

CN5
1 AC9V
2 GND

B5P-VH CN4
1 AC28V
2 GND
3 AC6V
4 −23V
5 AC6V

J1
1 A9V
2 A5V
3 AGND
4 AGND
5 AGND
6 A−5V
7 A−9V
8 DGND
9 DGND
10 D5V
11 D9V

J2
1 D5V
2 N.C.
3 D9V
4 DGND

PDE1232
1 2 3 4 5 6 7 8 9 10 11

MECHANISM
XA1516)

VO MECHANISM
SY (PXA1490)

CN107
A9V
A5V
AGND
AGND
AGND
A−5V
A−9V
DGND
DGND
D5V
D9V
B11B-PH-K-S

CN205
D5V
N.C.
D9V
DGND

21P
FLEXIBLE
CABLE
PDD1145

SENSV
:83)
OSC
FOCUS
TRACKING
LINEAR
F2
F1
D A
C B
E2
E1
1.25mmPITCH FPC

1 GNDA
2 SNSV
3 COUT
4 LD
5 GNDA
6
7 VA5V
8 A−5V
9 MD
10 FDR
11 TDR
12 TRT
13 FRT
14 GNDA
15 B
16 E2
17 E1
18 C
19 D
20 F1
21 VA5V
22 F2
23 A
24 GNDA
25 SRT
26 SDR

CN101
5597-26APB

HEAD BOARD
ASSY
(PWF1002)
(➡ SCH – 5)

SPD CON 1
REF V 2
FW REV 3
FG 4
N.C 5
XLDON 6
LD PW 7
3T 8
EFM 9
FCS CON 10
TRK CON 11
SLD CON 12
DGND 13
VSENS 14
TOCPOS 15
AGND 16
RF 17
HF 18
WBL 19
FE 20
TE 21
1.25mmPITCH FFC

CN106
HLEM21R-1

1 SPD CON
2 REF V
3 FW REV
4 FG
5 74/63
6 XLDON
7 LD PW
8 3T
9 EFM
10 FCS CON
11 TRK CON
12 SLD CON
13 N.C
14 VSENS
15 TOCPOS
16 AGND
17 RF
18 HF
19 WBL
20 FE
21 TE

CN201
HLEM21S-1

13P
FLEXIBLE
CABLE
PDD1144

H2
H3
FG
E MOTOR
36

1 FG−
2 FG+
3 VH+
4 H3−
5 H2+
6 H3+
7 VH−
8 H1+
9 H2−
10 H1−
11 W3
12 W2
13 W1
1.25mmPITCH FFC

CN102
HLEM13R-1

DGND 1
REC INH 2
EFM 3
XSAMPL 4
AGND 5
LDPW 6
SLDDRV 7

CN103 (TP1)
RKP-534

CN203
173981-6
1 AGND
2 AGND
3 XCDW
4 XCUP
5 XLOP
6 XLCL

CN208 (TP2
B5P-SHF-1
MN
MN
MN
MN
DG

F2−F1 1
E1−E2 2
STE 3
MSTE 4
TE 5
AGND 6
WBL 7
RWBL 8

CN104 (TP2)
RKP-535

1 LOAD
2 AGND
3 CLAMP
4 AGND

CN202
173981-4

CN209 (TP2
B6P-SHF-1
AT
AS
XE
MS
MS
DG

CN207 (TP201)
B6P-SHF-1AA
1 RF
2 TE
3 TIN
4 GNDA
5 FIN
6 FE

680
TOC BOARD ASSY
(PWM1774)
GP1A51HR
PDE1200
1 DGND
2 D5V
3 TOCPOS

CN105
173981-3

CONNECTOR ASSY
PDE1111

DC MOTOR
PXM1010
(LOADING)

DC MOTOR
PXM1010
(CLAMP)

CONNECTOR ASSY
PDE1110

S102 DSK1003
OPEN
CLOSE
S101 DSK1003

OVERALL WIRING
DIAGRAM
-1

SCH – 1

POWER SUPPLY BOARD ASSY
(PWZ2461)
(➡ SCH – 7)

B5P-VH
CN3
1 +A17
2 AUGND
3 –A17–

CN5
1 AC9V
2 GND

B5P-VH
CN4
1 AC28V
2 GND
3 AC6V
4 –23V
5 AC6V

J1
1 A9V
2 A5V
3 AGND
4 AGND
5 AGND
6 A–5V
7 A–9V
8 DGND
9 DGND
10 ØD5V
11 D9V

J2
1 D5V
2 N.C.
3 D9V
4 DGND
5 A–9V
6 A–5V
7 AGND
8 A+5V
9 A+9V

J3
1 XPFAIL
2 –27V
3 AC6V
4 AC6V
5 DA5V
6 DGND

PDE1233
1 D5V
2 N.C.
3 D9V
4 DGND
5 A–9V
6 A–5V
7 AGND
8 A+5V
9 A+9V

CN205

PDE1226
1 XPFAIL
2 –27V
3 AC6V
4 AC6V
5 DA5V
6 DGND

CN204
B6B-PH-K

SR
IN
OUT

DIGITAL OUT
OPTICAL 1
COAXIAL

DIGITAL IN
COAXIAL
OPTICAL 1
OPTICAL 2

PDE1218
1 DGND
2 ADDATA
3 DGND
4 LRCK
5 DGND
6 ADBCK
7 DGND
8 ADLRCK
9 DGND
10 ADPD

J301

CN802
1 DGND
2 ADDATA
3 DGND
4 LRCK
5 DGND
6 ADBCK
7 DGND
8 ADLRCK
9 DGND
10 ADPD

CN401
1 +A20
2 +A20

CN403
B3P-VH
1 +A10
2 CHASSIS
3 –A10

1 –A20
2 –A20

LINE (ANALOG)
OUT L R
IN L R

CN402

CN406
B7B-PH-K
1 MUTE
2 HPROUT
3 HPLOUT
4 AUGND
5 AU+12V
6 AUGND
7 AU–12V

21P
FLEXIBLE
CABLE
PDD1145

1.25mmPITCH FFC

CN201
HLEM21S-1
1 SPD CON
2 REF V
3 FW REV
4 FG
5 74/63
6 XLDON
7 LD PW
8 3T
9 EFM
10 FCS CON
11 TRK CON
12 SLD CON
13 N.C
14 VSENS
15 TOCPOS
16 AGND
17 RF
18 HF
19 WBL
20 FE
21 TE

SERVO · DIGITAL BOARD ASSY (PWM1717)
(1/2) SERVO SECTION : (➡ SCH – 2)
(2/2) DIGITAL SECTION : (➡ SCH – 3)

PDE1219
1 DGND
2 DATA
3 DGND
4 BCK
5 DGND
6 ADMCK
7 DGND
8 MCK
9 DGND
10 ACSL

J303

CN405
1 DGND
2 DATA
3 DGND
4 BCK
5 DGND
6 ADMCK
7 DGND
8 MCK
9 DGND
10 ACSL

AUDIO BOARD ASSY
(PWM1719)
(➡ SCH – 4)

CN801
AUGND
RVL IN
RVLOUT
AU – 12V
AUGND
AU + 12V
LVLOUT
LVL IN
AUGND

PDE1217
1 DGND
2 XDEEMP
3 XMUTE
4 XRESET
5 LDALT
6 RDALT
7 SHIFT
8 DACDT

J302

CN404
B8B-PH-K
1 DGND
2 XDEEMP
3 XMUTE
4 XRESET
5 LDALT
6 RDALT
7 SHIFT
8 DACDT

CN206
HLEM22S-1
1 MREQ
2 MACK
3 XRESET
4 FSCK
5 FSO
6 FSI
7 CWORK
8 UNLOCK
9 CUREQ
10 XRD
11 CUACK
12 CDR/CD
13 LR
14 XSOE
15 ATTLAT
16 RMDT
17 SR
18 DGND
19 D5V
20 AC6V
21 AC6V
22 –30V

J305
1 DOUT
2 DGND
3 D5V

PDE1253

J304
1 DGND
2 ORX
3 DGND
4 D5V

CN312
B3B-PH-K
1 DOUT
2 DGND
3 D5V

PDE1254

CN310
B4B-PH-K
1 DGND
2 ORX
3 DGND
4 D5V

ST BOARD AS
(PWZ2891)
(➡ SCH – 8)

1 DGND
2 DSCAN

22P
FLEXIBLE CABLE
PDD1156

1.25mmPITCH FFC

CN208 (TP202)
B5P-SHF-1AA
MNT3 1
MNT2 2
MNT1 3
MNT0 4
DGND 5

CN701
HLEM22R-1
1 MREQ
2 MACK
3 XRESET
4 FSCK
5 FSO
6 FSI
7 CWORK
8 UNLOCK
9 CUREQ
10 XRD
11 CUACK
12 CDR/CD
13 LR
14 XSOE
15 ATTLAT
16 RMDT
17 SR
18 DGND
19 D5V
20 AC6V
21 AC6V
22 –30V

CN203
173981-6
1 AGND
2 AGND
3 XCDW
4 XCUP
5 XLOP
6 XLCL

CN209 (TP203)
B6P-SHF-1AA
ATIPSYNC 1
ASYN 2
XECE 3
MSCK 4
MSO 5
DGND 6

CN202
173981-4
1 LOAD
2 AGND
3 CLAMP
4 AGND

CN207 (TP201)
B6P-SHF-1AA
1 RF
2 TE
3 TIN
4 GNDA
5 FIN
6 FE

J703
1 DSCAN
2 DATA3
3 DATA2
4 DATA1
5 DATA0
6 KS7
7 KS6
8 GND1

D20PWW0820E

1 DSCAN
2 DATA3
3 DATA2
4 DATA1
5 DATA0
6 KS7
7 KS6
8 GND1

SUB SW

DISPLAY SECTION

FUNCTION BOARD ASSY
(AWZ2464) (➡ SCH – 6)

J701
1 REMOTE
2 D5V
3 DGND

D20PWW0320G

REMOTE
D5V
DGND

REMOTE SENSOR SECTION

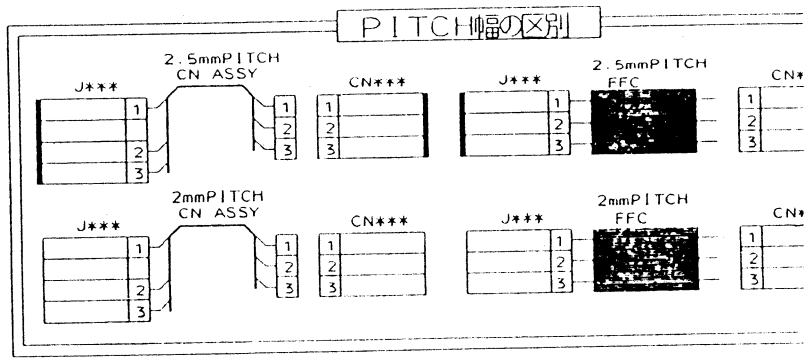
J702
1 DISLED
2 D5V
3 SKIP OFF
4 KS0
5 KS1
6 KS2
7 KS4
8 DGND
9 DATA0
10 DATA1
11 DATA2
12 DATA3

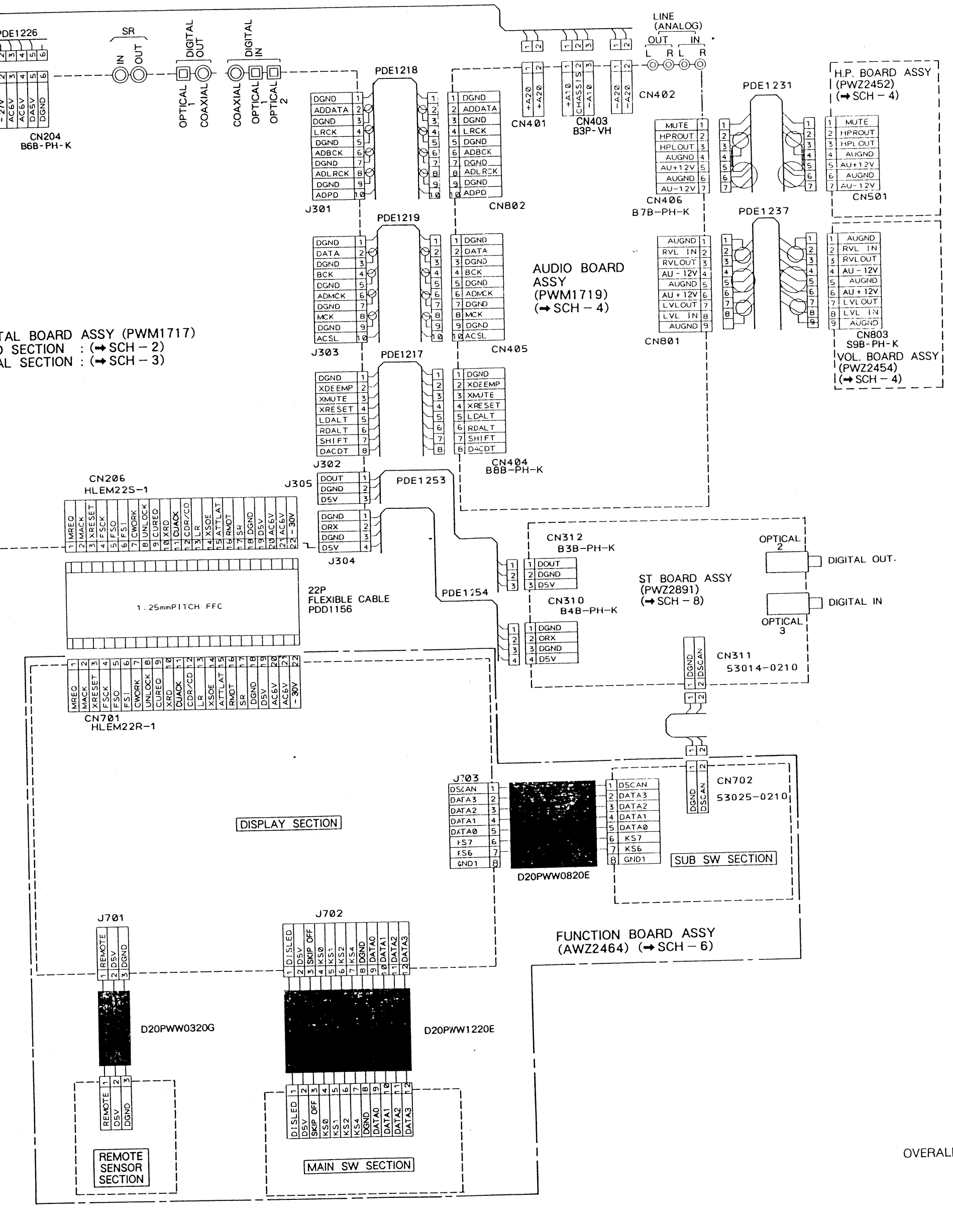
D20PWW1220E

DISLED
D5V
SKIP OFF
KS0
KS1
KS2
KS4
DGND
DATA0
DATA1
DATA2
DATA3

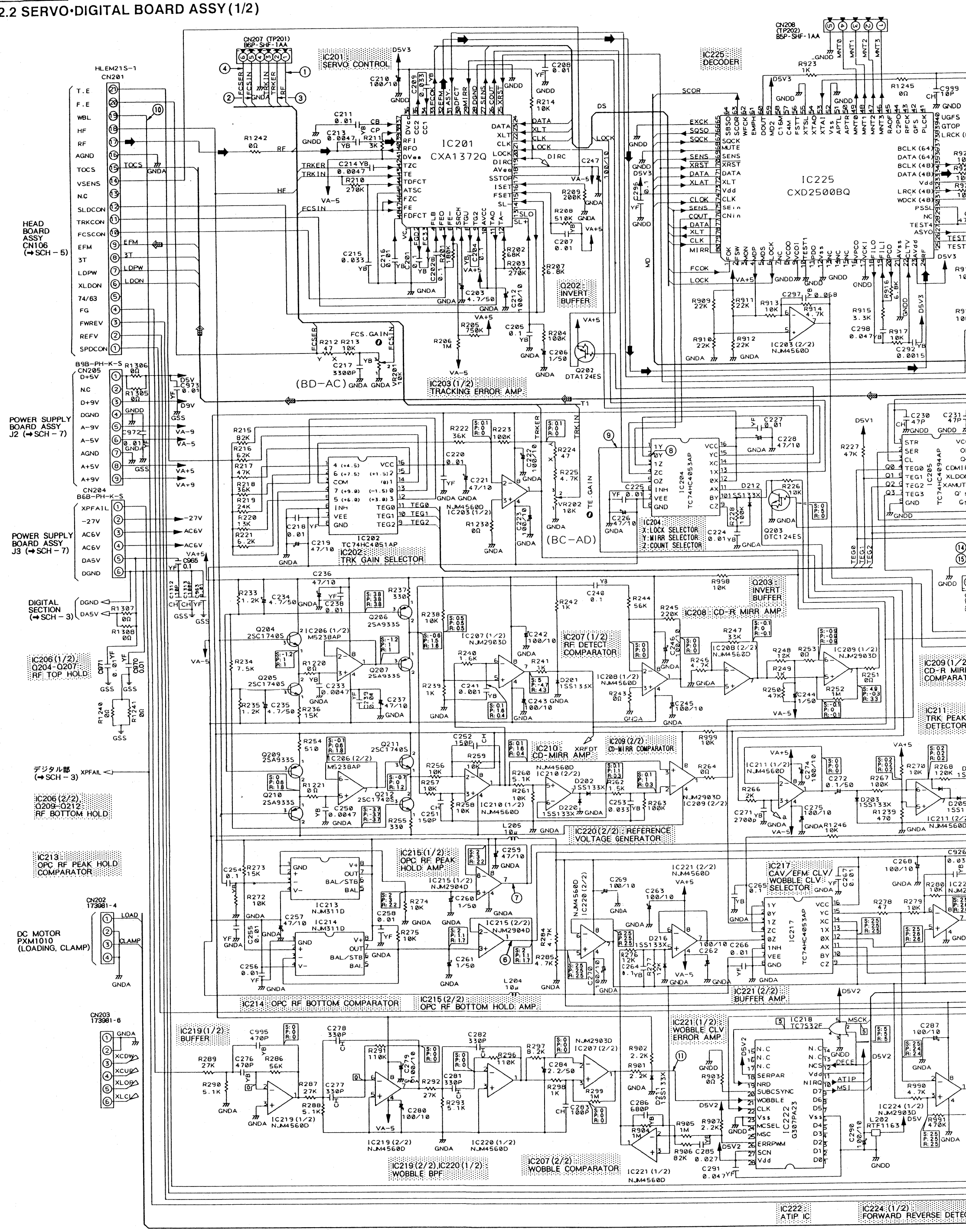
MAIN SW SECTION

SCH – 1


PITCH幅の区別
2.5mmPITCH CN ASSY
2.5mmPITCH FFC
2mmPITCH CN ASSY
2mmPITCH FFC
J***
CN***


PDE1226
CN204
B6B-PH-K
SR
IN
OUT
DIGITAL OUT
OPTICAL 1
COAXIAL
DIGITAL IN
COAXIAL
OPTICAL 1
OPTICAL 2
PDE1218
J301
CN802
PDE1219
J303
CN405
PDE1217
J302
CN404
B8B-PH-K
CN401
CN403
B3P-VH
LINE (ANALOG)
OUT
IN
L R L R
CN402
PDE1231
CN406
B7B-PH-K
PDE1237
CN801
H.P. BOARD ASSY (PWZ2452) (➡ SCH – 4)
CN501
CN803
S9B-PH-K
VOL. BOARD ASSY (PWZ2454) (➡ SCH – 4)
AUDIO BOARD ASSY (PWM1719) (➡ SCH – 4)
TAL BOARD ASSY (PWM1717)
) SECTION : (➡ SCH – 2)
AL SECTION : (➡ SCH – 3)
CN206
HLEM22S-1
J305
PDE1253
J304
22P
FLEXIBLE CABLE
PDD1156
PDE1254
1.25mmPITCH FFC
CN312
B3B-PH-K
CN310
B4B-PH-K
ST BOARD ASSY (PWZ2891) (➡ SCH – 8)
OPTICAL 2
DIGITAL OUT
DIGITAL IN
OPTICAL 3
CN311
53014-0210
CN701
HLEM22R-1
J703
D20PWW0820E
CN702
53025-0210
DISPLAY SECTION
SUB SW SECTION
J701
J702
D20PWW0320G
D20PWW1220E
FUNCTION BOARD ASSY (AWZ2464) (➡ SCH – 6)
REMOTE SENSOR SECTION
MAIN SW SECTION

2.2 SERVO·DIGITAL BOARD ASSY (1/2)



SCH-2 SERVO • DIGITAL BOARD ASSY (1/2)

SERVO • DIGITAL BOARD ASSY (1/2) (PWM1717)

● SERVO SECTION

➡ : PLAYBACK SIGNAL ROUTE

⇶ : REC SIGNAL ROUTE

IC225 DECODER

IC225 CXD2500BQ

IC226 ROM

IC226 PD6118C

IC227 RAM

IC227 LH5116-15

IC228 GGC1056 (UPD78323GJ-5BJ) MECHANISM CONTROL IC

DIGITAL SECTION (➡ SCH – 3)

IC203 (2/2) EFM CLV ERROR AMP.

IC204 : X:LOCK SELECTOR Y:MIRR SELECTOR Z:COUNT SELECTOR

IC205 SERIAL/PARALLEL CONVERTER

IC208 CD-R MIRR AMP.

IC209 (1/2) CD-R MIRR COMPARATOR

IC211 TRK PEAK DETECTOR

IC217 CAV/EFM CLV/ WOBBLE CLV SELECTOR

IC221 (2/2) BUFFER AMP.

IC221 (1/2) WOBBLE CLV ERROR AMP.

IC222 ATIP IC

IC223 SPINDLE CONTROL AMP.

IC224 (1/2) FORWARD REVERSE DETECTING CIRCUIT

IC224 (2/2) SPINDLE FG COMPARATOR

IC230 3 STATES BUFFER

IC231 (1/2) CLAMP MOTOR DRIVE

IC231 (2/2) LOADING MOTOR DRIVE

IC232 TC74HC4094AP

IC216 LD POWER BUFFER

Q201 SPINDLE STOP

Q203 INVERT BUFFER

Q213 MUTING BUFFER

Q214 INVERTER BUFFER

FUNCTION BOARD ASSY CN701 (➡ SCH – 6)

CN206 HLEM22S-1

CN208 (TP202) B5P-SHF-1AA

CN209 B6P-SHF-1AA

X201 : 16.00MHz

PSS1010 : X201

SERVO • DIGITAL BOARD ASSY (1/2) (PWM1717)
● SERVO SECTION

➡ : PLAYBACK SIGNAL ROUTE
⇶ : REC SIGNAL ROUTE

SCH – 2

IC226 : ROM
IC227 : RAM
IC236 : +5V REGULATOR
IC235 : RAM ENABLE BUFFER
IC229 : ADDRESS LATCH
IC234 : PARALLEL LATCH
IC233 : ADDRESS DECODER
IC232 : SERIAL/PARALLEL CONVERTER
IC203(2/2) : EFM CLV ERROR AMP
IC205 : SERIAL/PARALLEL CONVERTER
IC228 : MECHANISM CONTROL IC
IC230 : 3 STATES BUFFER
IC231 (1/2) : CLAMP MOTOR DRIVE
IC231 (2/2) : LOADING MOTOR DRIVE
IC216 : LD POWER BUFFER
IC223 : SPINDLE CONTROL AMP
IC224 (2/2) : SPINDLE FG COMPARATOR
Q201 : SPINDLE STOP
Q213 : MUTING BUFFER
Q214 : INVERTER BUFFER
Q208 : INVERT BUFFER

DIGITAL SECTION (➡ SCH – 3)
FUNCTION BOARD ASSY CN701 (➡ SCH – 6)

Note :
S : STOP state
P : PLAY state
R : REC state
STOP state unless otherwise noted.

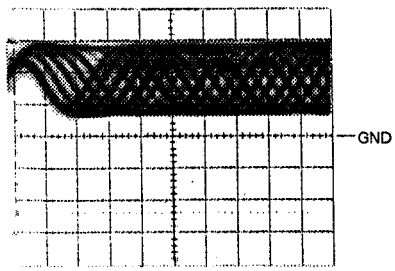
SERVO • DIGITAL BOARD ASSY (1/2)

SCH-2

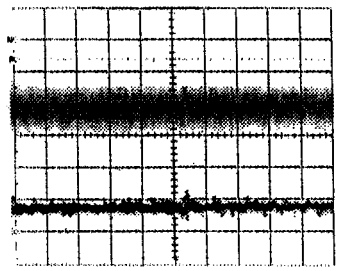
• Waveformes at SERVO·DIGITAL board assy (1/2)

• Measuring condition : DC input unless otherwise noted.

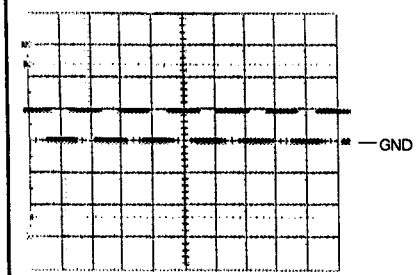
① CN207 (TP201) pin 1 (RF)
(during PLAY)
V range : 500mV/div.
H range : 0.5μsec/div.



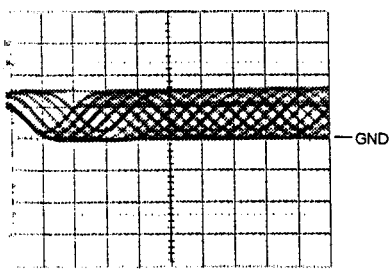
③-2 CN207 (TP201) pin 2 (TRKER)
(TEST TRK. CLOSE)
Upper : Filter is absent.
Lower : Filter is present.
V range : 200mV/div.
H range : 2msec/div.



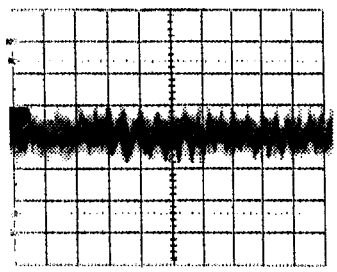
⑤-1 IC224 pin 7
(during PLAY at inner periphery)
V range : 5V/div.
H range : 2msec/div.



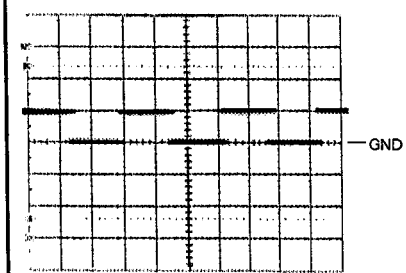
② CN207 (TP201) pin 7 (HF)
(during PLAY)
V range : 1V/div.
H range : 0.5μsec/div.



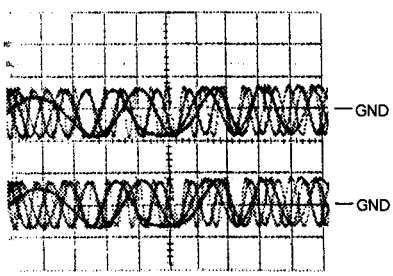
④-1 CN207 (TP201) pin 6 (FCSER)
(TEST TRK. OPEN)
V range : 200mV/div.
H range : 2msec/div.



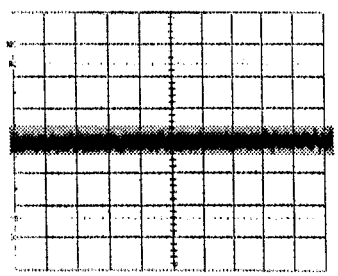
⑤-2 IC224 pin 7
(during PLAY at outer periphery)
V range : 5V/div.
H range : 2msec/div.



③-1 CN207 (TP201) pin 2 (TRKER)
(TEST TRK. OPEN)
Upper : Filter is absent.
Lower : Filter is present.
V range : 2V/div.
H range : 2msec/div.

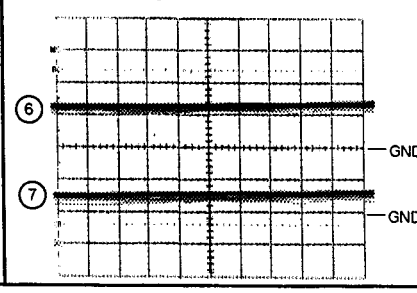


④-2 CN207 (TP201) pin 6 (FCSER)
(TEST TRK. CLOSE)
V range : 200mV/div.
H range : 2msec/div.



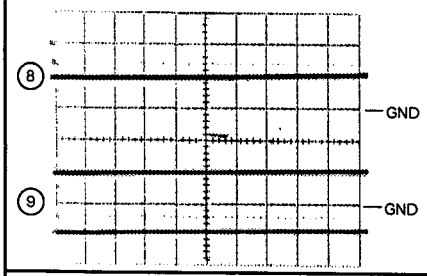
⑥ IC215 pin 7

⑦ IC215 pin 7
(during PLAY)
V range : 2V/div.
H range : 0.5msec/div.



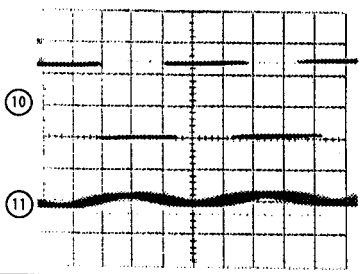
(8) IC204 pin 2 (CD MIRR)

(9) IC204 pin 1 (CD-R MIRR)
(during PLAY with defective CD)
V range : 5V/div.
H range : 0.5msec/div.



(10) CN201 pin 3

(11) IC222 pin 21 (CD-R PLAY)
V range : 2V/div.
H range : 10μsec/div.



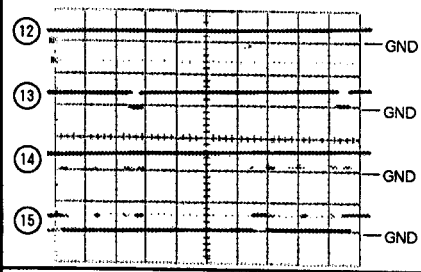
(12) CN209(TP203) pin 2

(13) CN209(TP203) pin 3

(14) CN209(TP203) pin 4

(15) CN209(TP203) pin 5

(CD-R PLAY)
V range : 10V/div.
H range : 2msec/div.



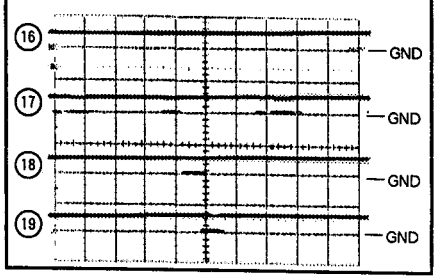
(16) IC230 pin 3

(17) IC230 pin 5

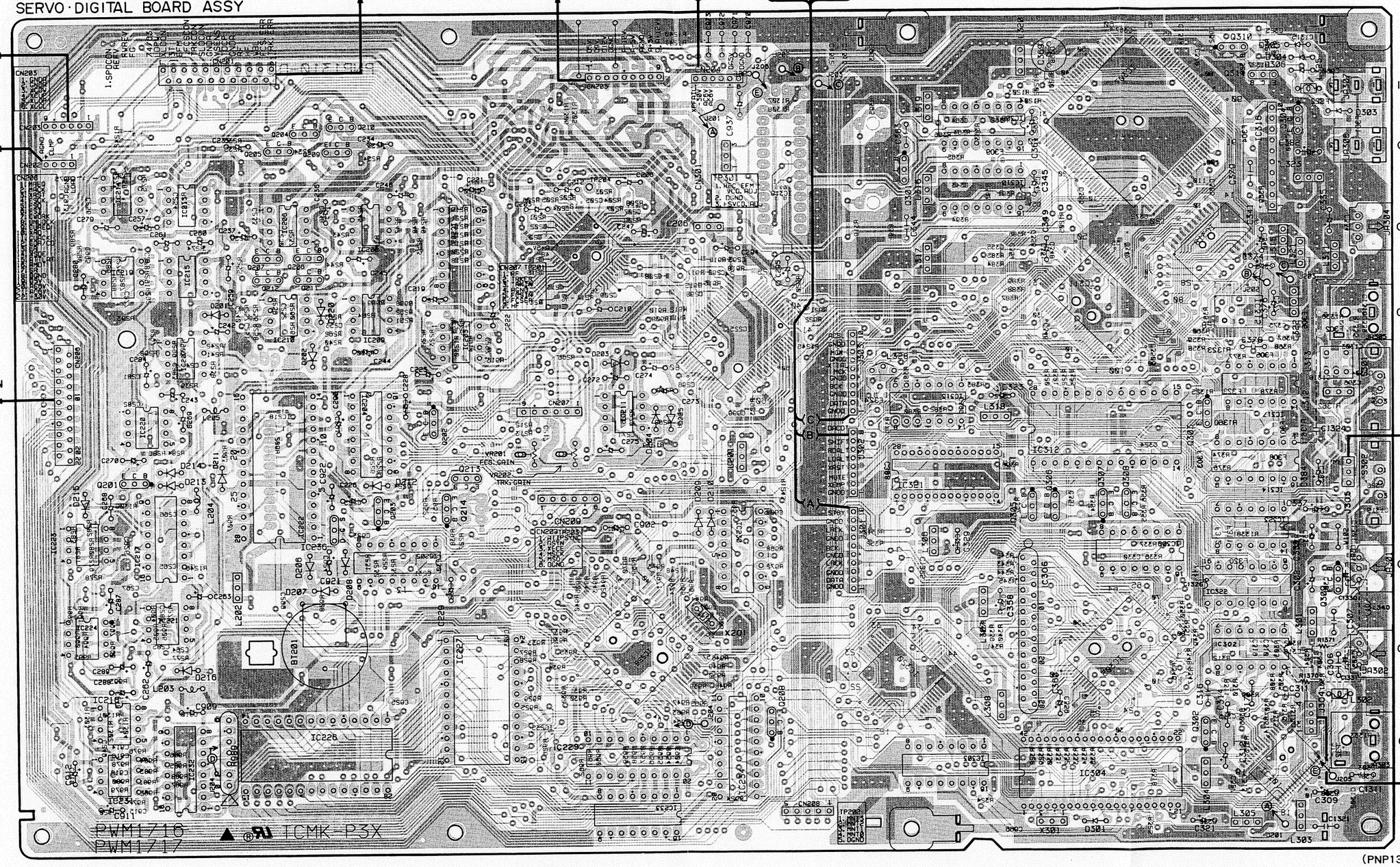
(18) D209 anode

(19) D210 anode

V range : 10V/div.
H range : 2msec/div.



SERVO · DIGITAL BOARD ASSY



VR201 VR202
TP201 TP203 TP204

TP301 TP202

Q201
IC213 — IC217
IC219 IC207
IC223 IC220 IC221
IC224 IC231 IC232

Q204 — Q207
Q209 — Q212 Q203
IC206 IC236 IC208
IC210 IC226 IC209
IC218 IC222 IC204 IC205 IC227

Q202 Q214 Q213
IC202
IC203

IC201
IC211 IC228
IC229
IC233

Q208
IC230 IC219
IC234

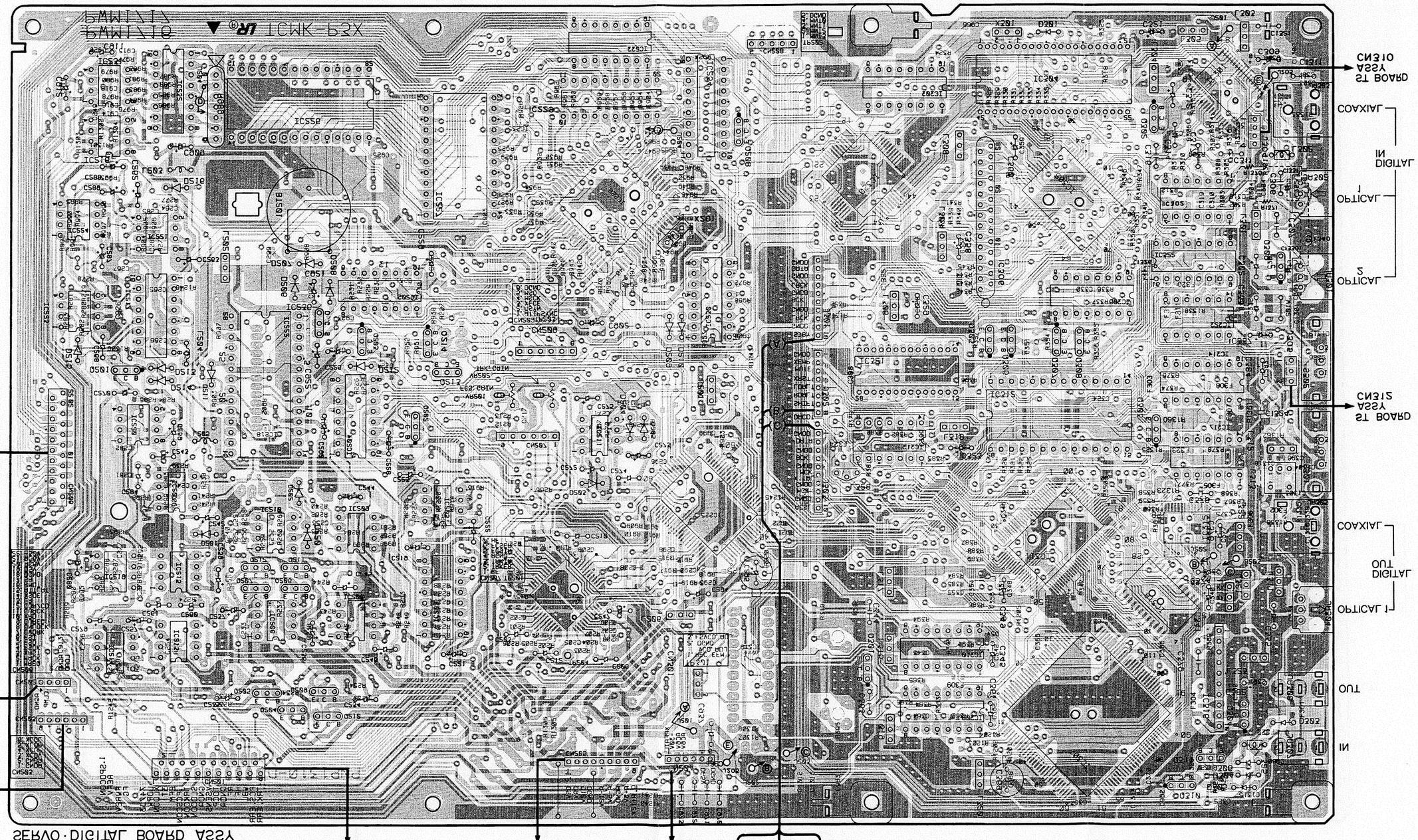
Q301
IC313 IC310
IC321 IC306
IC303

IC308
IC312
IC304

Q305 — Q308
IC309

IC307 Q302 Q303 Q310 Q304 Q309
IC305 IC311 IC318 IC315 IC317 IC316
IC314 IC323
IC322 IC302

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.


SERVO·DIGITAL BOARD ASSY
CN108
HEAD BOARD ASSY
CN107
POWER SUPPLY BOARD ASSY
CN805 CN804 CN802
AUDIO BOARD ASSY
CN101
FUNCTION BOARD ASSY
CN103
DC MOTOR (LOADING)
S101, S102
COAXIAL
OPTICAL
DIGITAL
IN
OUT
COAXIAL
OPTICAL
DIGITAL
OUT
TO BOARD ASSY CN151
TO BOARD ASSY CN152
PCB – 1
PDR-09

• Waveformes at SERVO•DIGITAL board assy (2/2)

• Measuring condition : DC input unless otherwise noted.

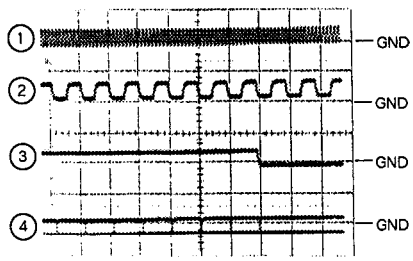
① J303 pin 8 (MCK)

② J303 pin 4 (BCK)

③ J303 pin 6 (LRCK)

④ J303 pin 2 (DATA)

(during PLAY)
V range : 10V/div.
H range : 0.5 µsec/div.



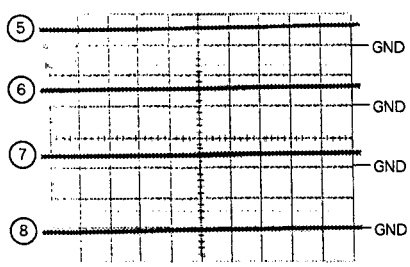
⑤ J302 pin 5 (LLAT)

⑥ J302 pin 6 (RLAT)

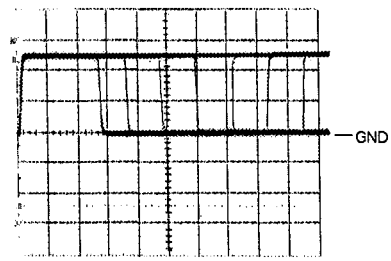
⑦ J302 pin 7 (SIFT)

⑧ J302 pin 8 (DADT)

(during PLAY)
V range : 10V/div.
H range : 2msec/div.



⑨ IC319 pin 4 (EFM)
(during REC)
V range : 2V/div.
H range : 0.2 µsec/div.



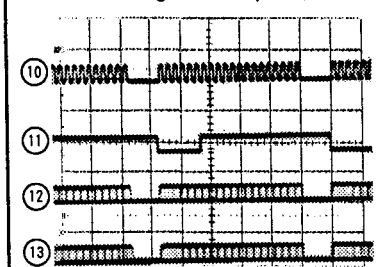
⑩ IC307 pin 116 (BCK)

⑪ IC307 pin 117 (WCK)

⑫ IC307 pin 118 (DOL)

⑬ IC307 pin 119 (DOR)

(during REC, DIN)
V range : 10V/div.
H range : 0.5 µsec/div.



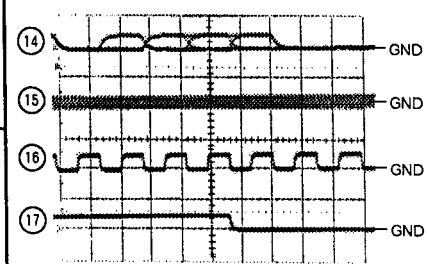
⑭ J301 pin 2 (DATA)

⑮ J301 pin 4 (MCK)

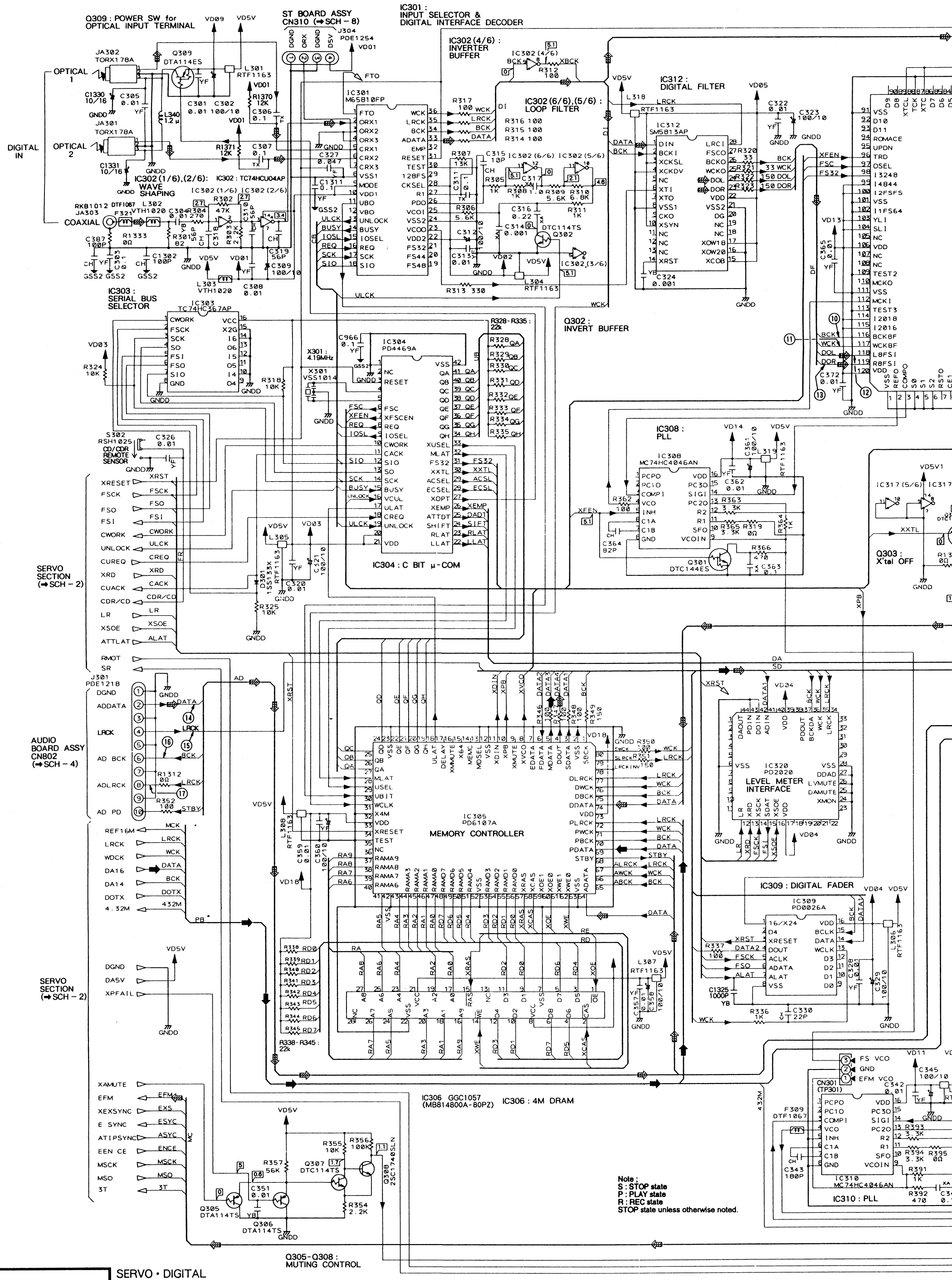
⑯ J301 pin 6 (BCK)

⑰ J301 pin 8 (LRCK)

(during REC)
V range : 10V/div.
H range : 1 µsec/div.



2.3 SERVO•DIGITAL BOARD ASS'Y (2/2)



SCH-3 SERVO • DIGITAL BOARD ASSY (2/2)

SERVO • DIGITAL ASSY (2/2) (PWI
● DIGITAL SECTION

IC307
PD6093A
FS CONVERETER

IC315 :
JITTER CLEANER

IC315
M65811FP

IC317 (2/6) :
LOOP FILTER

IC316 : VCO

IC316
PCX1021

IC312 :
DIGITAL FILTER

IC312
5813AP

IC314 :
MASTER CLOCK
SELECTOR

IC314
TC74HC153AP

Q303 :
X'tal OFF

IC317 (3/6),(6/6) :
INVERTER BUFFER

IC313 : TC74HC04AP

IC313 (3/6)-(5/6) :
INVERTER BUFFER

IC313 (1/6),(6/6) :
INVERTER BUFFER

IC318 GGF9002
(HM6264ALFP-12)

IC318 : 64k SRAM

IC320
PD2020
LEVEL METER
INTERFACE

IC309 : DIGITAL FADER

IC309
PD0026A

IC310
MC74HC4046AN

IC310 : PLL

IC311
LC89583
EFM ENCODER

IC321
TC9231N

IC321
DIGITA
INTERF
ENCOD

IC322 :
DIGITAL OUT
SELECTOR

IC322
TC74HC153AP

IC323 (1/6) - (6/6) :
INVERTER BUFFER

IC323 (1/6)
TC74HC04AP

IC319 :
EFM CONTROL

IC319
TC7S08F

R1201-R1204 :
100

IC228 (MECH. CON) 64pin

unless otherwise noted.

SERVO • DIGITAL ASSY (2/2) (PWM1717)
• DIGITAL SECTION

SCH - 3

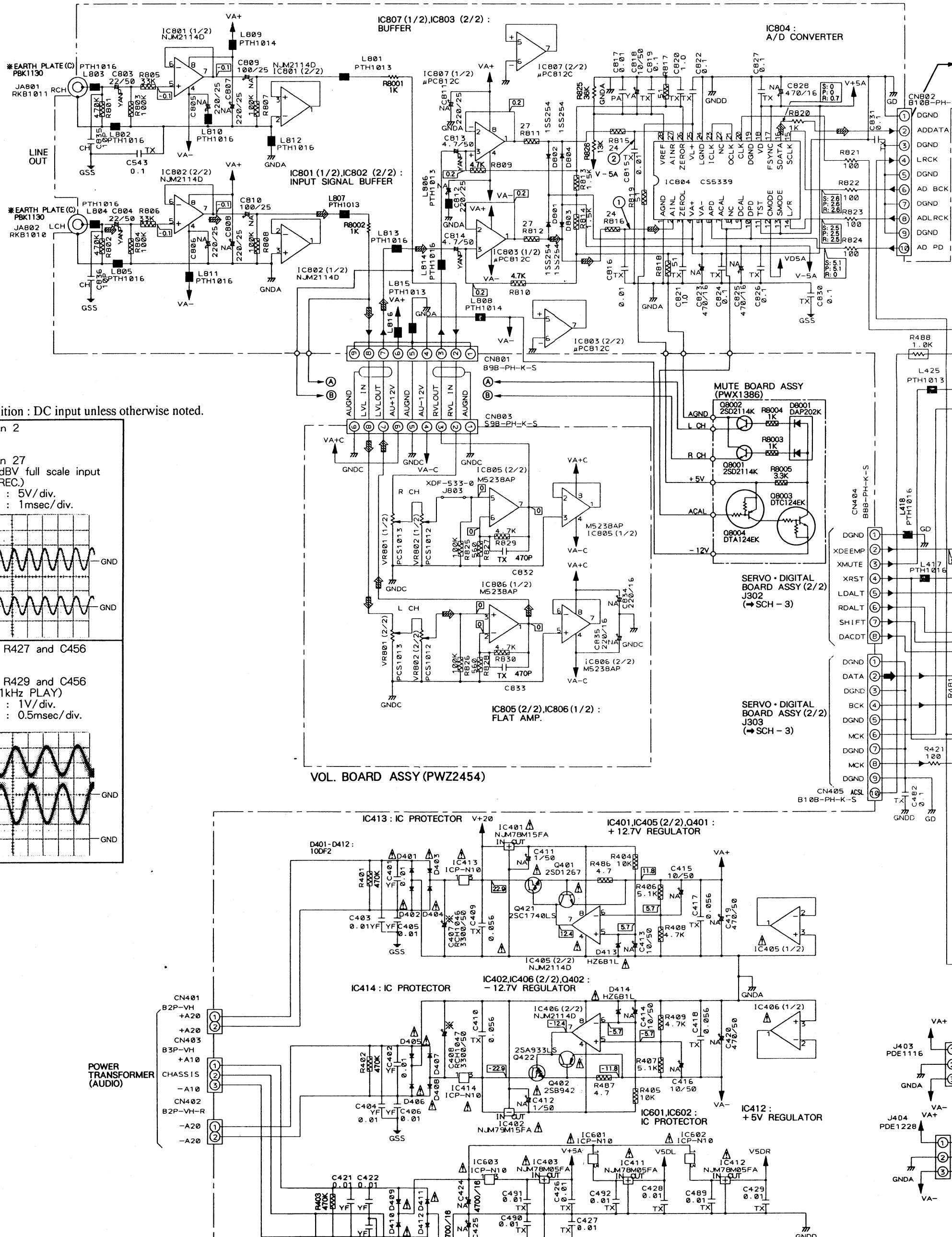
➡ : PLAYBACK SIGNAL ROUTE
▨ : REC SIGNAL ROUTE

IC315 : JITTER CLEANER
IC315 M65811FP
IC317 (2/6) : LOOP FILTER
IC316 : VCO
IC316 PCX1021
IC317 (2/6)
Q304 DTA114ES
Q304 : VCO POWER SW
IC317 (1/6) TC74HCU04AP
IC317 (1/6) : INVERTER BUFFER
IC307 PD6093A CONVERETER
IC314 : MASTER CLOCK SELECTOR
IC314 TC74HC153AP
IC313 (3/6) IC313 (2/6) IC313 (5/6)
IC317 (3/6) IC317 (6/6)
IC317 (3/6),(6/6) : INVERTER BUFFER
IC313 : TC74HC04AP
IC313 (3/6)-(5/6) : INVERTER BUFFER
IC313 (1/6),(6/6) : INVERTER BUFFER
IC318 GGF9002 (HM6264ALFP-12)
IC318 : 64k SRAM
IC311 LC89583 EFM ENCODER
IC319 TC7S08F
IC319 : EFM CONTROL
IC228 (MECH. CON) 64pin
IC321 TC9231N
IC321 : DIGITAL INTERFACE ENCODER
IC322 TC74HC153AP
IC322 : DIGITAL OUT SELECTOR
IC323 (6/6) IC323 (5/6) IC323 (4/6) IC323 (1/6) TC74HC04AP
IC323 (1/6) - (6/6) : INVERTER BUFFER
R1201-R1204 : 100
J303 PDE1219 — AUDIO BOARD ASSY CN405 (➡ SCH - 4)
J302 PDE1217 — AUDIO BOARD ASSY CN404 (➡ SCH - 4)
J305 PDE1253 — ST BOARD ASSY CN312 (➡ SCH - 8)
JA304 TOTX178 — DIGITAL OUT OPTICAL
S301 RSH1025 — DIGITAL OUT OFF
JA305 RKB1012 — DIGITAL OUT COAXIAL
JA306 PKN1004 — SR OUT
JA307 PKN1004 — SR IN
SR JACK
アースパン (J) PBK1130

SERVO • DIGITAL BOARD ASSY (2/2)

SCH-3

2.4 AUDIO BOARD, H.P. BOARD, VOL. BOARD AND MUTE BOARD ASSEMBLIES



• Measuring condition : DC input unless otherwise noted.

1 IC804 pin 2

2 IC804 pin 27
(1kHz 6dBV full scale input during REC.)
V range : 5V/div.
H range : 1msec/div.

3 Between R427 and C456

4 Between R429 and C456
(During 1kHz PLAY)
V range : 1V/div.
H range : 0.5msec/div.

SCH-4 AUDIO BOARD ASSY, H.P. BOARD ASSY, VOL. BOARD ASSY, MUTE BOARD ASSY

IC804 :
A/D CONVERTER

SERVO・DIGITAL
BOARD ASSY (2/2)
J301
(➡SCH－3)

CN802
B10B-PH-K-S

AUDIO BOARD ASSY (PWM1719)

IC417 (4/6),(6/6),
IC419 (4/4) :
INVERTER BUFFER

IC419 (1/4),(2/4),(3/4) :
MASTER CLOCK SELECTOR

IC417 (5/6) :
CLOCK OSC

IC417 (1/6) - (3/6) :
INVERTER BUFFER

H.P. BOARD AS

MUTE BOARD ASSY
(PWX1386)

SERVO・DIGITAL
BOARD ASSY (2/2)
J302
(➡SCH－3)

SERVO・DIGITAL
BOARD ASSY (2/2)
J303
(➡SCH－3)

Q406 :
INVERTER
BUFFER

Q403-Q405,
Q407,Q409 :
INVERTER BUFFER

IC407,IC408 :
D/A CONVERTER

IC409,IC410,Q413-Q416 :
LOW-PASS FILTER

IC401,IC405 (2/2),Q401 :
+12.7V REGULATOR

IC601,IC602 :
IC PROTECTOR

IC412 :
+5V REGULATOR

IC411 :
+5V REGULATOR

Q411 :
DEEMPHASIS SW

Q412 :
DEEMPHASIS SW

Q408,Q410 :
INVERTER BUFFER

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-N10, MFD BY ROHM CO., LTD. FOR IC413, IC414 AND IC601－IC604.

GITAL
SSY (2/2)
3)

: PLAYBACK SIGNAL ROUTE
: REC SIGNAL ROUTE

SCH – 4

AUDIO BOARD ASSY (PWM1719)

IC417 (4/6),(6/6),
IC419 (4/4) :
INVERTER BUFFER

IC419 (1/4),(2/4),(3/4) :
MASTER CLOCK SELECTOR

IC417 (1/6) - (3/6) :
INVERTER BUFFER

IC417 (6/6)

Q403-Q405,
Q407,Q409 :
INVERTER BUFFER

IC407,IC408 :
D/A CONVERTER

IC409,IC410,Q413-Q416 :
LOW-PASS FILTER

Q408,Q410 :
INVERTER BUFFER

Q411 :
DEEMPHASIS SW

Q412 :
DEEMPHASIS SW

Q417 :
ZERO DETECTING
ATTENUATOR

Q418 :
ZERO DETECTING
ATTENUATOR

Q419,Q420 :
OUTPUT MUTE

H.P. BOARD ASSY (PWZ2452)

IC501 :
HEADPHONE AMP.

Q501,Q502 :
HEADPHONE MUTE

VR501
PHONES LEVEL

PHONES

LINE
OUT

Note ;
S : STOP state
P : PLAY state
R : REC state
STOP state unless otherwise noted.

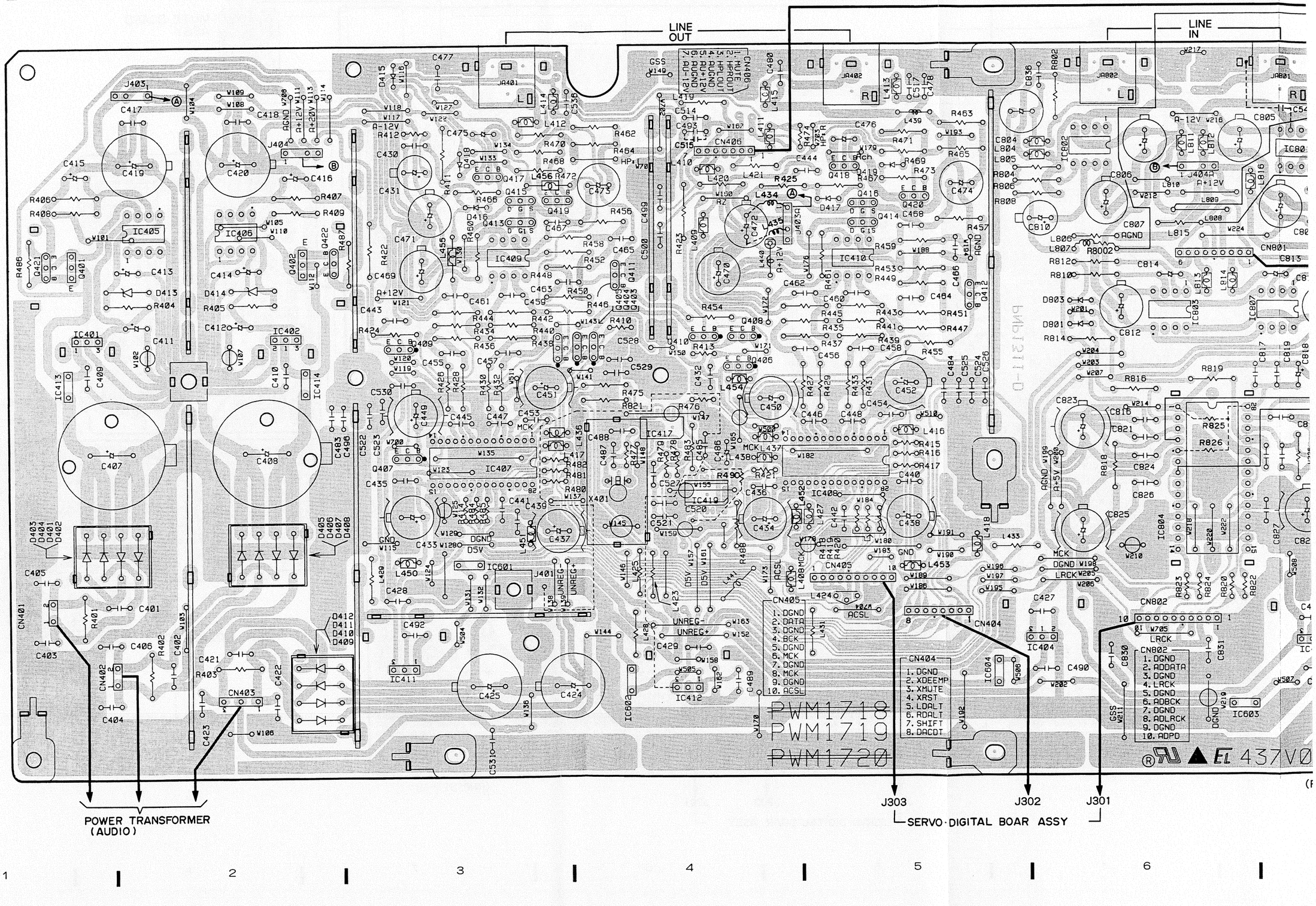
AUDIO BOARD ASSY,
H.P. BOARD ASSY,
VOL. BOARD ASSY,
MUTE BOARD ASSY

SCH-4

AUDIO BOARD ASSY

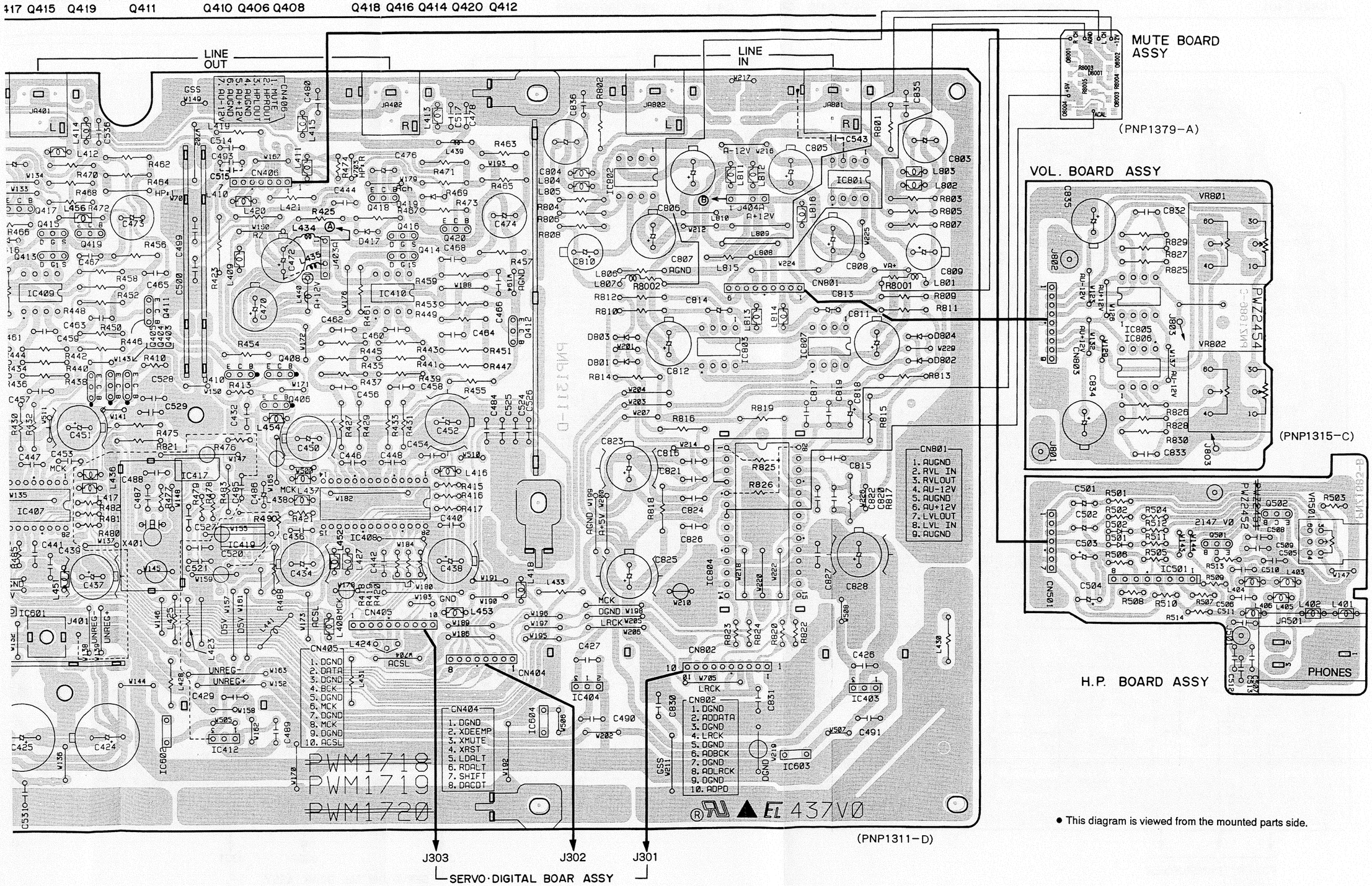
IC413 IC401 IC405 IC406 IC402 IC414 IC411 IC601 IC407 IC409 IC413 IC602 IC419 IC410 IC603 IC4

Q421 Q401 Q402 Q422 Q407 Q409 Q417 Q415 Q419 Q411 Q403–Q405 IC417 IC412 Q410 Q406 Q408 IC408 Q418 Q416 Q414 Q420 Q412 IC604 IC404 IC802 IC803 IC804 IC807 IC8

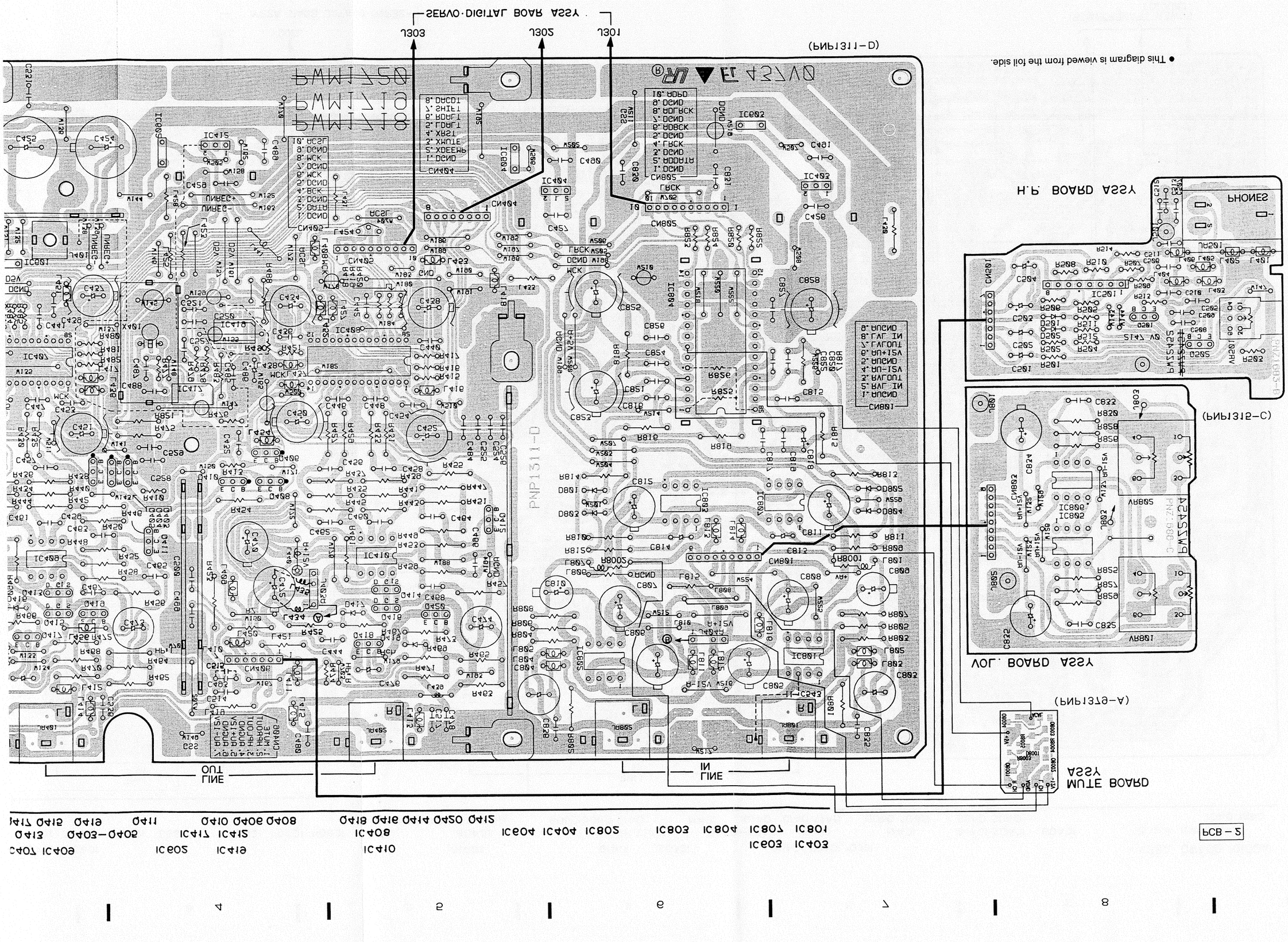


407 IC409 IC602 IC419 IC410 IC603 IC403
Q413 Q403–Q405 IC417 IC412 IC408 IC604 IC404 IC802 IC803 IC804 IC807 IC801
417 Q415 Q419 Q411 Q410 Q406 Q408 Q418 Q416 Q414 Q420 Q412

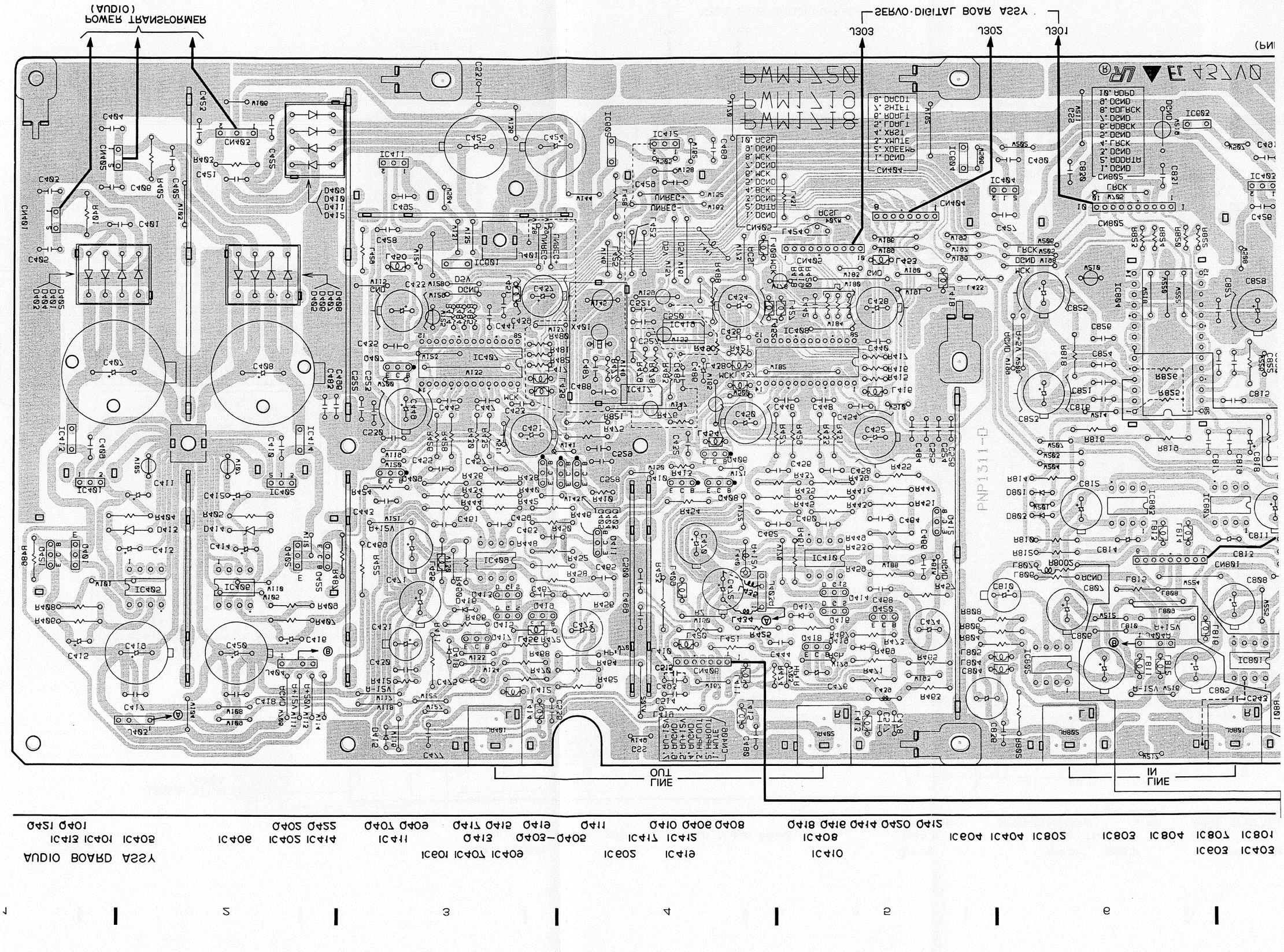
PCB – 2



- This diagram is viewed from the mounted parts side.



• This diagram is viewed from the foil side.

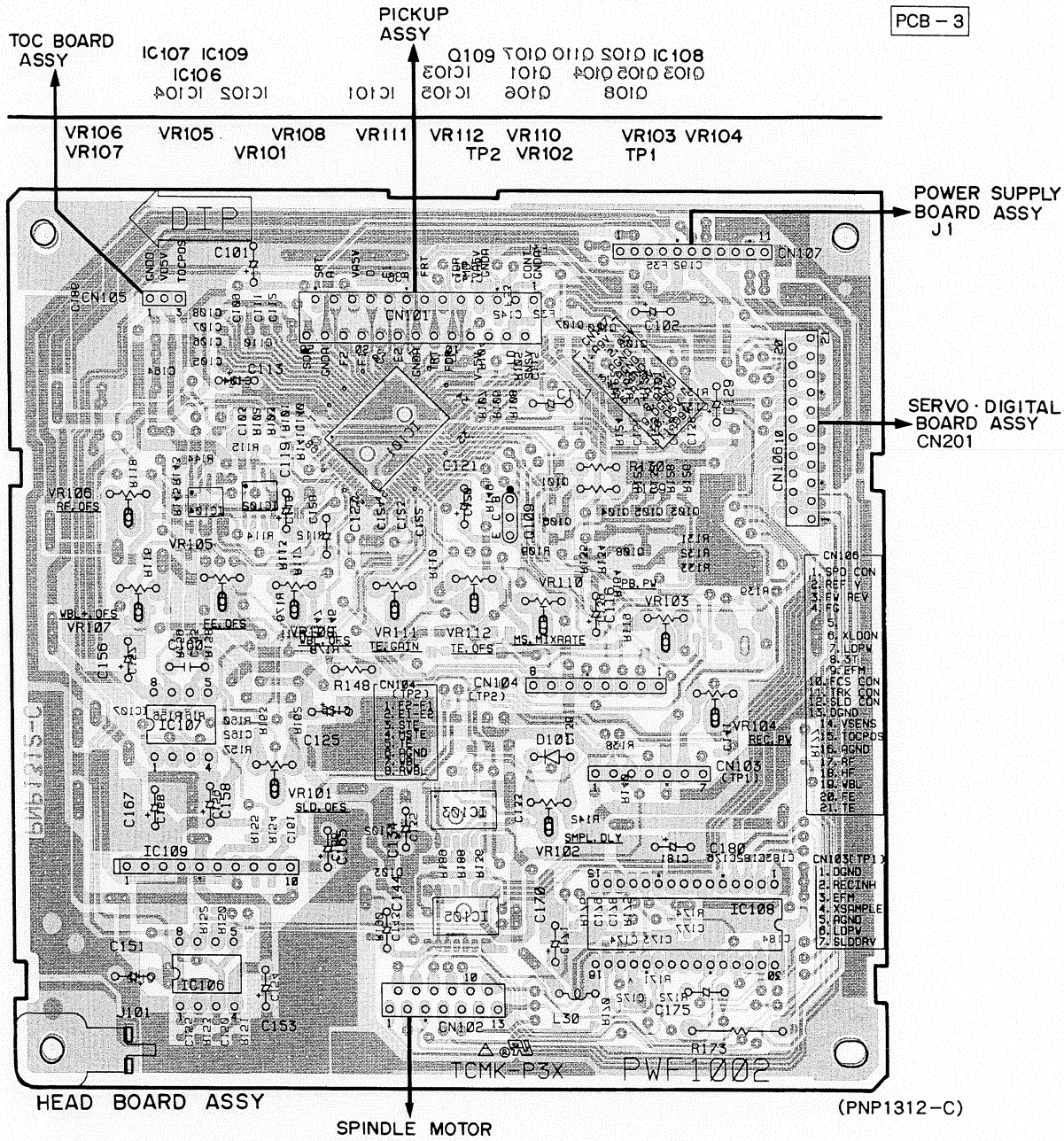

POWER TRANSFORMER (AUDIO)
SERVO·DIGITAL BOARD ASSY
CN801
CN802
CN803
LINE OUT
LINE IN
PNP1311-D
AUDIO BOARD ASSY

2.5 HEAD BOARD , TOC BOARD AND PICKUP ASSEMBLIES

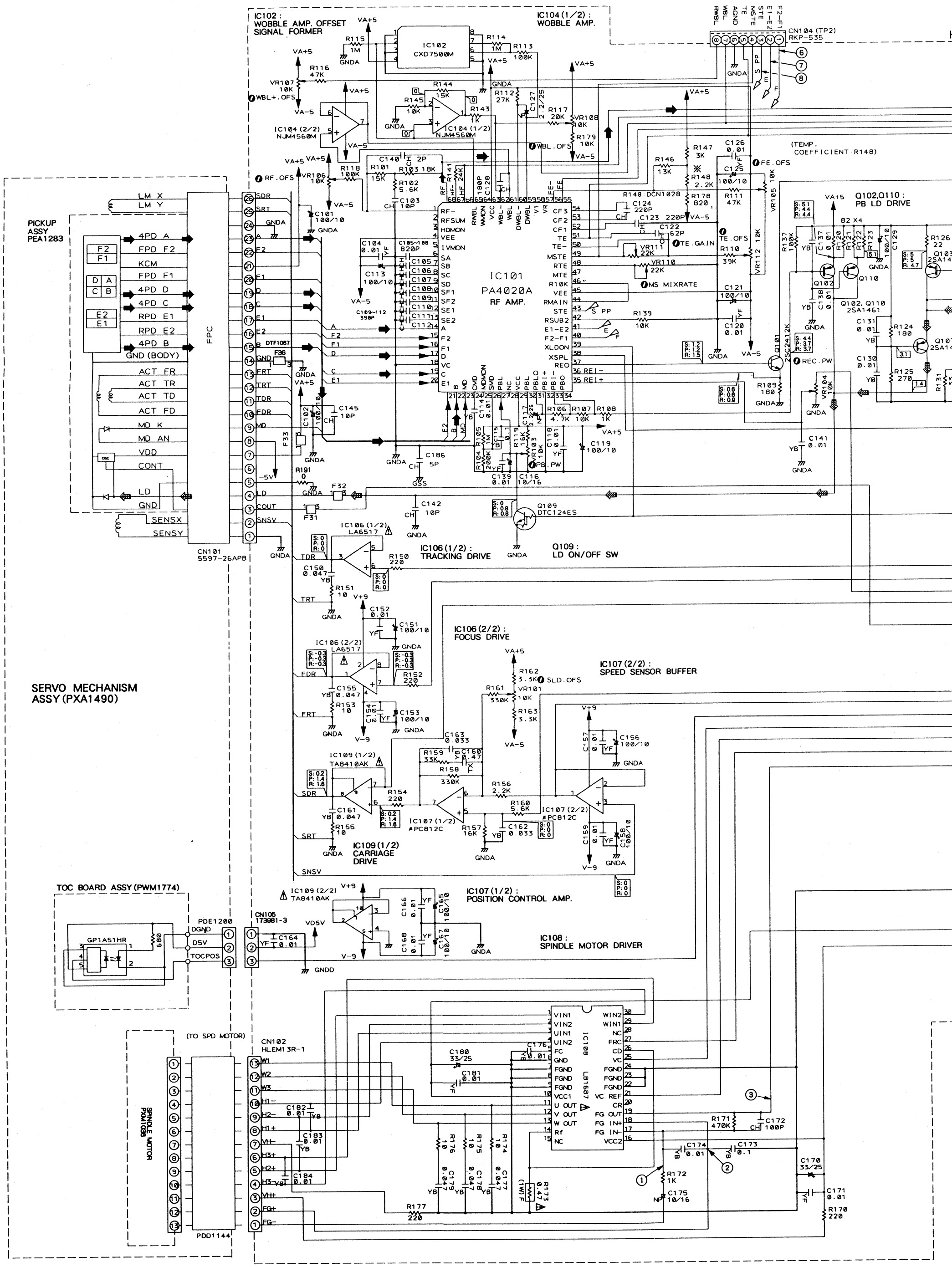
PCB - 3

- This diagram is viewed from the gray colored foil side.
- This PCB is double sided.

2.5 HEAD BOARD , TOC BOARD AND PICKUP ASSEMBLIES



- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.


IC102 : WOBBLE AMP. OFFSET SIGNAL FORMER
IC102 CXD7500M
IC104 (1/2) : WOBBLE AMP.
IC104 (2/2) NJM4560M
IC104 (1/2) NJM4560M
CN104 (TP2) RKP-535
RWBL
WBL
AGND
TE
MSTE
STE
E1-E2
F2-F1
PICKUP ASSY PEA1283
4PD A
FPD F2
KCM
FPD F1
4PD D
4PD C
RPD E1
RPD E2
4PD B
GND (BODY)
ACT FR
ACT TR
ACT TD
ACT FD
MD K
MD AN
VDD
CONT
LD
GND
SENSX
SENSY
CN101 5597-26APB
FPC
DTF1087
IC101 PA4020A RF AMP.
RF.OFS
WBL+.OFS
WBL.OFS
FE.OFS
TE.OFS
TE.GAIN
MS MIXRATE
REC.PW
PB.PW
SLD.OFS
(TEMP. COEFFICIENT:R148)
R148:DCN1028
Q102,Q110 : PB LD DRIVE
Q101 2SC2412K
Q102, Q110 2SA1461
Q103 2SA14
SERVO MECHANISM ASSY (PXA1490)
IC106 (1/2) LA6517
IC106 (1/2) : TRACKING DRIVE
Q109 : LD ON/OFF SW
Q109 DTC124ES
IC106 (2/2) : FOCUS DRIVE
IC106 (2/2) LA6517
IC109 (1/2) TA8410AK
IC109 (1/2) CARRIAGE DRIVE
IC107 (1/2) PC812C
IC107 (2/2) PC812C
IC107 (2/2) : SPEED SENSOR BUFFER
IC109 (2/2) TA8410AK
IC107 (1/2) : POSITION CONTROL AMP.
IC108 : SPINDLE MOTOR DRIVER
TOC BOARD ASSY (PWM1774)
PDE1200
GP1A51HR
CN105 173981-3
CN102 HLEM13R-1
(TO SPD MOTOR)
SPINDLE MOTOR PXM1036
PDD1144
IC108 LB1687
SCH-5
HEAD BOARD ASSY, TOC BOARD ASSY, PICKUP ASSY

HEAD BOARD ASSY (PWF1002)

➡ : PLAYBACK SIGNAL ROUTE
▨ : REC SIGNAL ROUTE

Note :
S : STOP state
P : PLAY state
R : REC state
STOP state unless otherwise noted.

SCH – 5

CN104 (TP2)
RKP-535
RWBL, WBL, AGND, TE, NSTE, STE, E1-E2, F2-F1

Q102,Q110 : PB LD DRIVE

Q103-Q108,Q101 : REC LD DRIVE

(TEMP. COEFFICIENT R129, R130)

R129, R130 : PCN1027

IC103 (1/4),(4/4) : INVERTER BUFFER

IC103 (2/4),(3/4) : SAMPLE PULSE FORMER

IC103 (4/4)

IC103 (3/4)

IC103 (1/4)

IC103 (2/4)
TC74HC00AF

IC105
TC74HC08AF
(1/4), (2/4), (3/4), (4/4)

IC105 : BUFFER

CN103 (TP1)
RKP-534
DGND, REC INH, EFM, XSAMPL, AGND, LDPW, SLD DRV

SERVO • DIGITAL BOARD ASSY (1/2)
CN201
(➡ SCH – 2)

CN106
HLEM21R-1

CN107
B11B-PH-K-S

POWER SUPPLY BOARD ASSY
J1
(➡ SCH – 7)

HEAD BOARD ASSY (PWF1002)

➡ : PLAYBACK SIGNAL ROUTE
▨ : REC SIGNAL ROUTE

Note ;
S : STOP state
P : PLAY state
R : REC state
STOP state unless otherwise noted.

SCH – 5

Q103-Q108,Q101 :
REC LD DRIVE

(TEMP. COEFFICIENT R129, R130)

R129, R130 : PCN1027

R127 22
R128 22
R129 120 ※
R130 120 ※
C132 0.1
Q104 2SA1461
Q105 YB 2SA1461
Q106 2SA1461
Q108 2SA1461
R135 1.3K
R164 510
R134 3.6K
R132 33
R133 33

IC103 (1/4),(4/4) :
INVERTER BUFFER

VD5V
100/10 C134
C135 0.01 YF
IC103 (4/4)
R136 1K
C133 22P
IC103 (1/4)
R188 1.3K
R189 3.6K
R142 20K
D101 1SS133X
IC103 (3/4)
C136 220P CH
VR102 22K ※
SMPL . DLY
GNDD
GNDA

IC103 (2/4),(3/4) :
SAMPLE PULSE
FORMER

R140 47K
R138 4.7K
IC103 (2/4)
TC74HC00AF

VA+5
R149 47K

D102 DAN202K
D103 DAN202K

IC105
TC74HC08AF
(3/4)
C143 0.1 YF
C144 10/50
R190 1K
(1/4)
(2/4)
(4/4)
IC105 : BUFFER

CN103 (TP1)
RKP-534
1 DGND
2 REC INH
3 EFM
4 XSAMPL
5 AGND
6 LDPW
7 SLD DRV
21 TE
20 FE
19 WBL
18 HF
17 RF
16 AGND
15 TOCPOS
14 VSENS
13 DGND
12 SLD CON
11 TRK CON
10 FCS CON
9 EFM
8 3T
7 LDPW
6 LDON
5 N.C
4 FG
3 FW REV
2 REF V
1 SPD CON

SERVO • DIGITAL BOARD ASSY (1/2) CN201 (➡ SCH – 2)

CN106
HLEM21R-1

CN107
B11B-PH-K-S
1 A9V
2 A5V
3 AGND
4 AGND
5 AGND
6 A-5V
7 A-9V
8 DGND
9 DGND
10 D5V
11 D9V

V+9
VA+5
F35 DTF1064
VA-5
V-9
L30 10μ VD5V

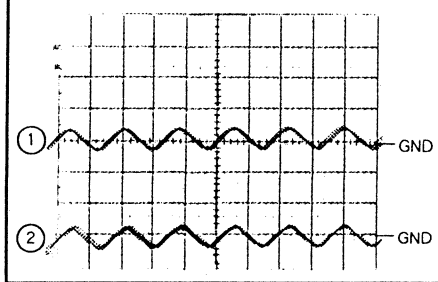
POWER SUPPLY BOARD ASSY J1 (➡ SCH – 7)

• Waveformes at HEAD board assy

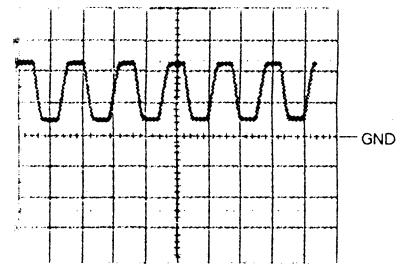
• Measuring condition :
DC input unless otherwise noted.

(1) IC108 pin 17

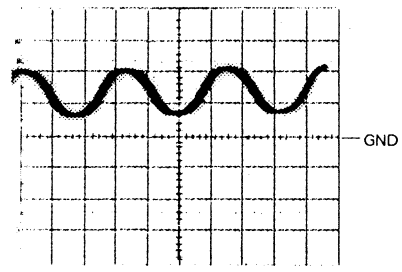
(2) IC108 pin 18
(during PLAY)
V range : 1V/div.
H range : 2msec/div.



(3)-1 IC108 pin 19
(during PLAY at innermost)
V range : 2V/div.
H range : 2msec/div.

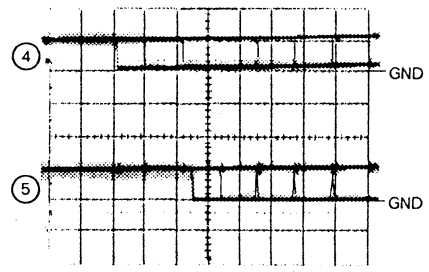


(3)-2 IC108 pin 19
(during PLAY at outermost)
V range : 2V/div.
H range : 2msec/div.



(4) IC103 pin 8

(5) IC103 pin 6
(during REC)
V range : 5V/div.
H range : 0.2μsec/div.

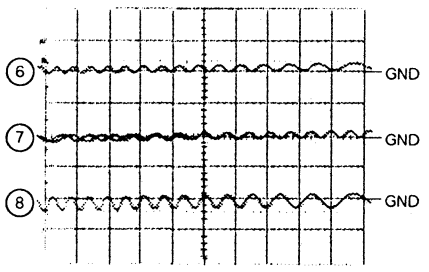


(6) CN104 pin 1

(7) CN104 pin 2

(8) CN104 pin 3

(TEST TRK OPEN)
V range : 1V/div.
H range : 2msec/div.



HEAD BOARD ASSY,
TOC BOARD ASSY,
PICKUP ASSY

SCH-5

2.6 FUNCTION BOARD ASSY

FUNCTION BOARD ASSY (PWZ2464)

Note ;
Voltages are at STOP state.

Q701-Q704 :
BUFFER

IC702 :
RESET

IC703 :
EXPANDER for
LED DRIVE

• MAIN SW SECTION

SSY (1/2)

SCH – 6

Q704 :
R

Note ;
Voltages are at STOP state.

IC702 :
RESET

IC702 M51957AL

VCC1

R704 22K
C704 47/16
10K
C705 YF
C706 0.022
R706 1K
R705 2.2/50
GND1

Q701
2SC1740S

D707~D710 1SS254
D707 D708 D709 D710

R724 390
D706 SLH-34VC35H3-S
D705 SLH-34VC35H3-S
D704 SLH-34VC35H3-S
D703 SLH-34VC35H3-S

C708 47/16
GND1

VDD 16
RESET 15
SI 14
OUT7 13
OUT6 12
OUT5 11
OUT4 10
XOE 9

OPTICAL1 S716 RSG1030
EJECT S720 RSG1030
S724 RSG1030
OPTICAL2 S717 RSG1030
STOP S721 RSG1030
COAXIAL S718 RSG1030
PLAY S722 RSG1030
ANALOG S719 RSG1030
S723 RSG1030

R726 390

TEST MODE
GND1

DISLED
D5V
SKIP OFF
KS0
KS1
KS2
KS4
DGND
DATA0
DATA1
DATA2
DATA3

J702
D20PWW1220E

J703
D20PWW0820E

D SCAN
DATA3
DATA2
DATA1
DATA0
KS7
KS6
GND1

ST BOARD ASSY
CN311 (➡SCH – 8)
DGN1
DSCAN
CN702
53025-0210

REC S725 RSG1030
PAUSE S726 RSG1030
SCAN + S727 RSG1030
SCAN – S728 RSG1030
RECMUTE S729 RSG1030

• SUB SW SECTION

ECTION
210S
711
DISP
OFF

GND3
D716 680 R727
SLH-34VC35H3-S
SKIP OFF

SKIP ON/OFF S705 PSG1009
INDEX NO. S710 RSG1030

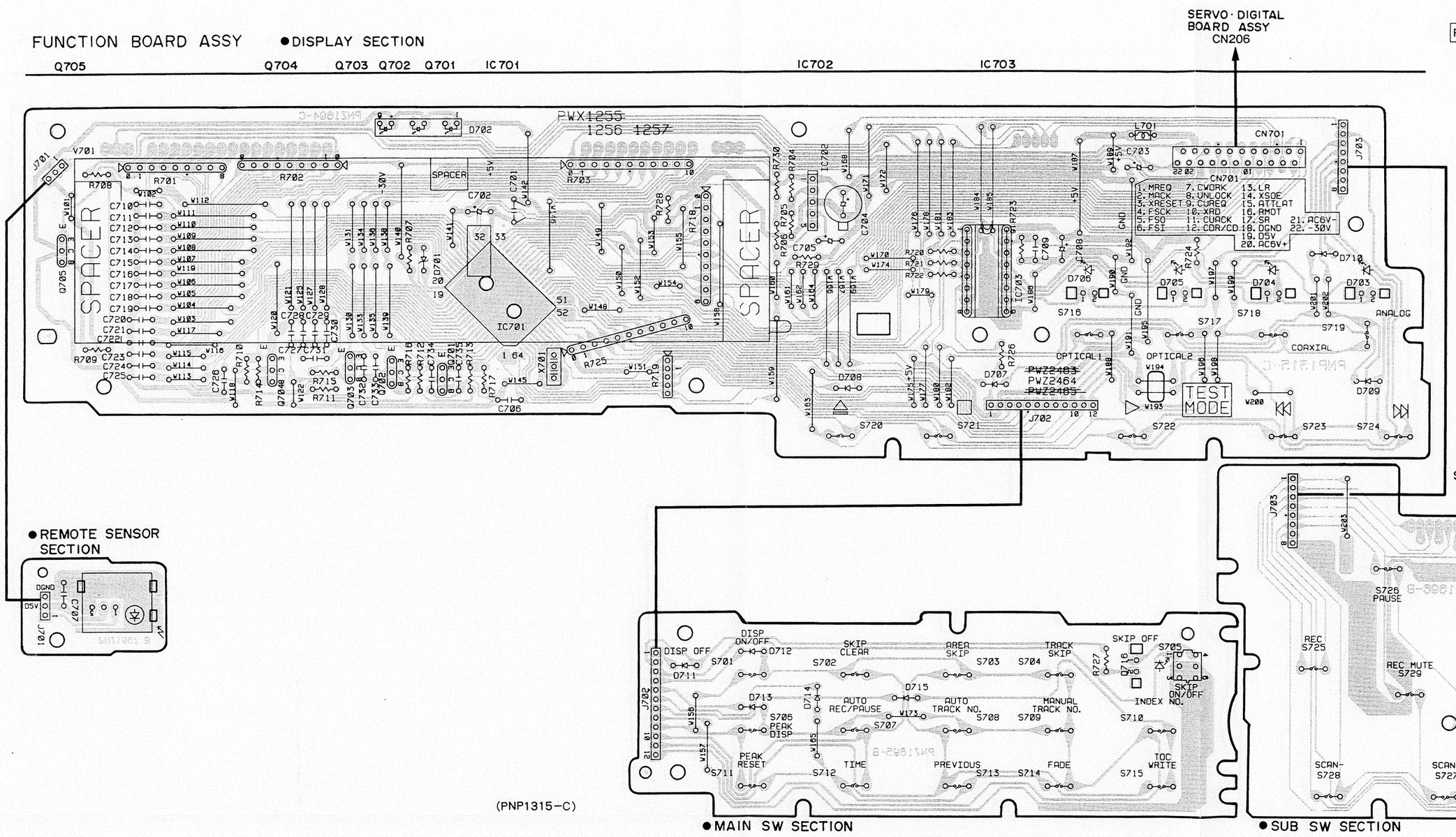
DISP ON/OFF S701 RSG1030
SKIP CLEAR S702 RSG1030
AREA SKIP S703 RSG1030
TRACK SKIP S704 RSG1030
PEAK DISP S706 RSG1030
AUTO REC/PAUSE S707 RSG1030
AUTO TRACK NO. S708 RSG1030
MANUAL TRACK NO. S709 RSG1030
PEAK RESET S711 RSG1030
TIME S712 RSG1030
PREVIOUS S713 RSG1030
FADE S714 RSG1030
TOC WRITE S715 RSG1030

D712 1SS254
D713 1SS254
D714 1SS254
D715 1SS254

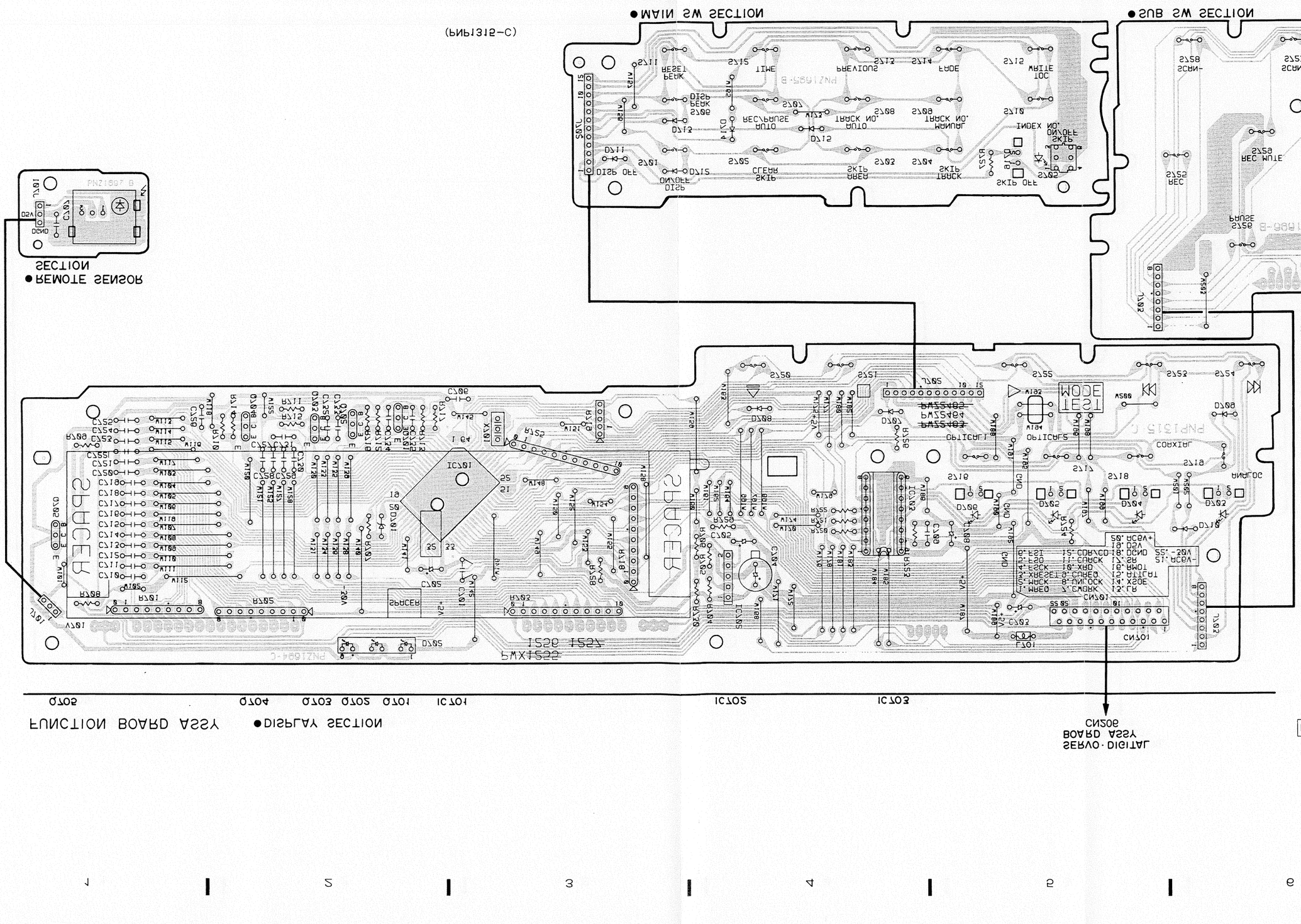
FUNCTION
BOARD ASSY

SCH-6

FUNCTION BOARD ASSY ●DISPLAY SECTION



● This diagram is viewed from the mounted parts side.

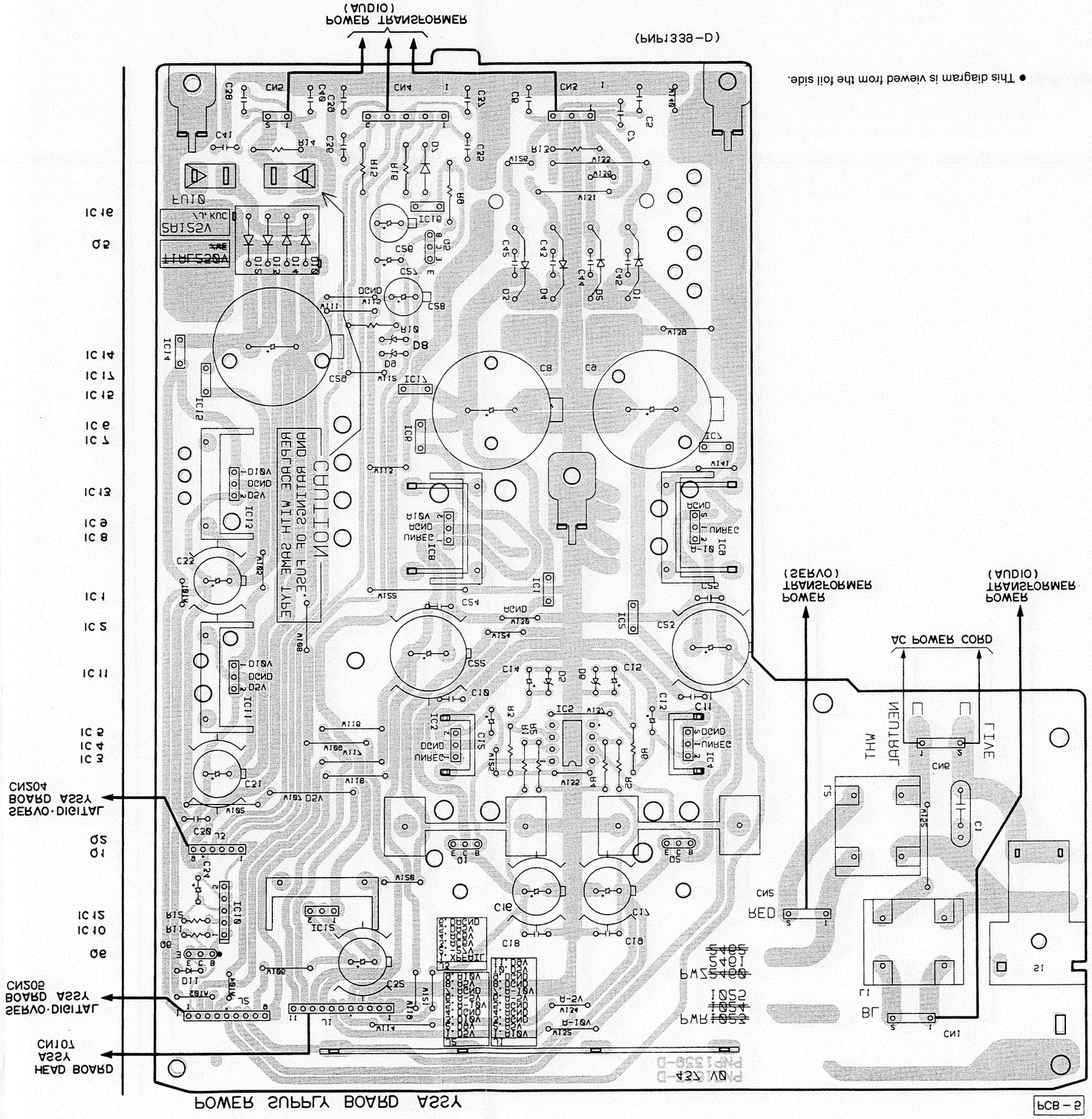

● REMOTE SENSOR SECTION
● MAIN WS SECTION
● SUB WS SECTION
TO ST BOARD ASSY CN131
FUNCTION BOARD ASSY ● DISPLAY SECTION
CN308 BOARD ASSY SERVO · DIGITAL
PCB – A
● This diagram is viewed from the foil side.
(C-2161HN)
PNZ1607 B
PNZ1585-B
PNZ1586-B
PNZ1584-C
PNP1315 C
2PHASE

2.7 POWER SUPPLY BOARD ASSY

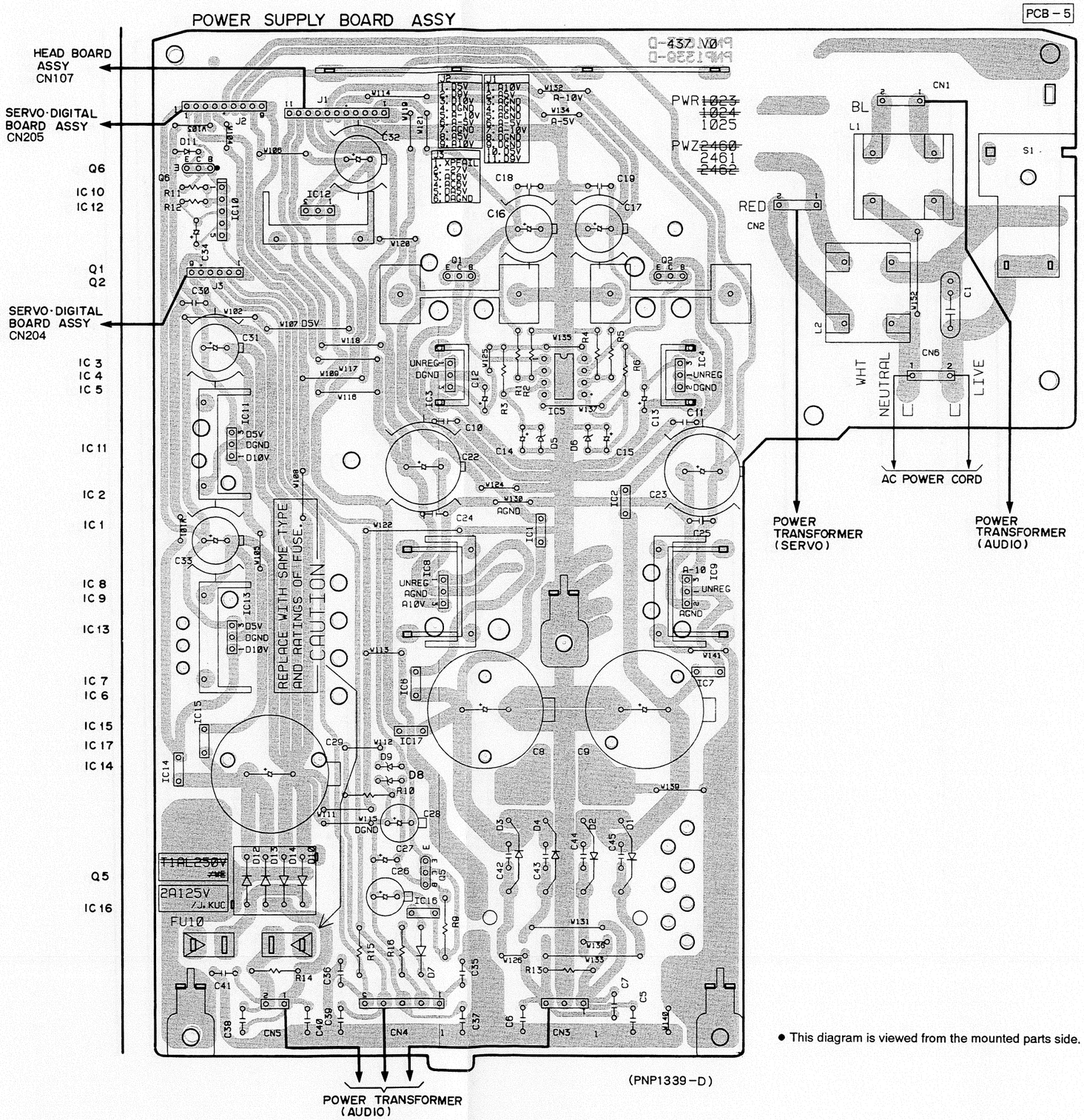
PDR - 09

(P-BB1NA)

● This diagram is viewed from the foil side.



2.7 POWER SUPPLY BOARD ASSY



● This diagram is viewed from the mounted parts side.

PION-04343 / DRUCK 16

SCH - 7

POWER SUPPLY BOARD ASSY (PWZ2461)

POWER TRANSFORMER (AUDIO) PTT1293

AUDIO BOARD ASSY (⇒SCH - 4)

CN403 VHR-3N (GRN, BLK, BLU)

CN401 VHR-2N (BRN, RED)

CN402 VHR-2N-R (ORG, YEL)

CN1 B2P3-VH-E

WHT / PAR

CN6 RKC-061 (NEUTRAL, LIVE)

AC120V 60Hz

AC POWER CORD PDG1015

L1 PTL1009

L2 PTL1002

C1 0.01 VCG-044

S1 PSA1004 POWER

CN2 B2P3-VH-R

B3P-VH CN3 (BRN, BLK, RED) VHR-3N

C5 0.01 YF, C6 0.01 YF, C7 0.01 YF

C44 0.01, C43 0.01, C45 0.01, C42 0.01

D1~D4 : 31DF2-FC5

D1, D2, D3, D4

R13 300K

C8 6800/25 RCH1016

C18 0.047 TX

IC1 : IC PROTECTOR

IC1 ICP-N20

IC17 ICP-N10

IC12 NJM7805FA

C32 220/50 NA

IC3 NJM7809FA

C12 1/50 NA

IC3,IC5(1/2),Q1 : +5V REGULATOR

Q1 2SD1267

R1 4.3K, R3 10K, C16 1000/16 NA, C18 0.047 TX

IC5 (1/2) NJM2114D

R2 6.2K, D5 HZ3BLL, C14 33/25 NA

C9 6800/25 RCH1016, C11 0.047 TX

R4 6.2K, D6 HZ3BLL, C15 33/25 NA, C17 1000/16 NA, C19 0.047 TX

Q2 2SB942

IC5 (2/2) NJM2114D

IC2 ICP-N20

C13 1/50 NA

R6 10K

IC4 NJM7909FA

IC4,IC5(2/2),Q2 : −5V REGULATOR

IC6 ICP-N15

IC8 NJM7809FA

C22 470/50 NA, C24 0.047 TX

IC8 : +9V REGULATOR

IC2,IC6,IC7 : IC PROTECTOR

C23 470/50 NA, C25 0.047 TX

IC7 ICP-N10

IC16 ICP-N10

IC9 NJM7909FA

IC9 : −9V REGULATOR

C35 1.0 TX

B5P-VH CN4 (GRN, BLK, BLU, VLT, RED) VHR-5N

D7 1SR35-100A, Q5 2SA1283

R9 1.5K (1/2) FR, D9 MTZJ7.5A

Q5 : −27V REGULATOR

R16 300K, C26 100/50, C27 47/35, D8 MTZJ27A, C28 100/50, R10 3.9K

R15 300K

C36 1.0 TX, C37 1.0 TX, C39 0.01 YF

IC14,IC15 : IC PROTECTOR

IC11 NJM7805FA

IC15 ICP-N20

IC11,IC13 : +5V REGULATOR

D10, D12~D14 : 11DF2

IC13 NJM7805FA

C31 1000/16 NA

IC14 ICP-N20

B2P-VH CN5 (ORG, YEL) VHR-2N

C38 0.01 YF, FU10 : 2A VEK1019, R14 300K, C40 0.01 YF, C41 0.01 YF

D10, D12, D13, D14

C29 6800/25 RCH1016, C30 0.047 TX, C31 1000/16 NA

GND

POWER TRANSFORMER (SERVO) PTT1292

IC10 : SYSTEM RESET

IC10 M51957AL

D11 1SS254, Q6 DTA144ES, R11 10K, R12 5.6K, C34 1/50

Q6 : INVERTER BUFFER

GSS

Note ; Voltages are at STOP state.

J1 PDE1232 → HEAD BOARD ASSY CN107 (⇒SCH - 5)

A+9V, A+5V, AGND, AGND, AGND, A−5V, A−9V, DGND, D+5V, D+9V

J2 PDE1233 → SERVO • DIGITAL BOARD ASSY (1/2) CN205 (⇒SCH - 2)

D+5V, N.C, D+9V, DGND, A−9V, A−5V, AGND, A+5V, A+9V

J3 PDE1226 → SERVO • DIGITAL BOARD ASSY (1/2) CN204 (⇒SCH - 2)

XPFAIL, −27V, AC6V, AC6V, DA5V, DGND

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-N15, MFD BY ROHM CO., LTD. FOR IC6.

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-N20, MFD BY ROHM CO., LTD. FOR IC1, IC2, IC14 AND IC15.

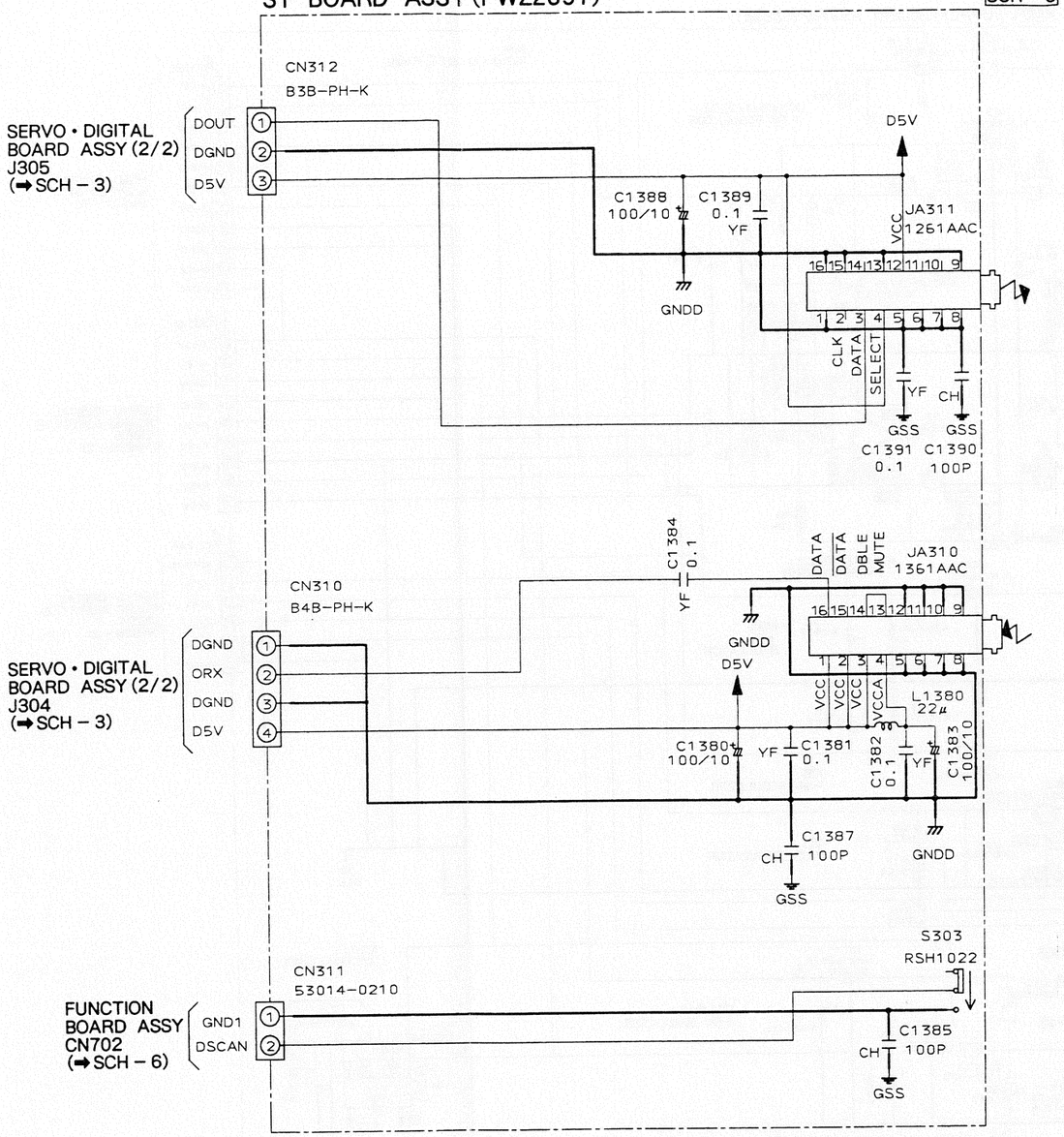
CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-N10, MFD BY ROHM CO., LTD. FOR IC7, IC16 AND IC17.

SCH-7 POWER SUPPLY BOARD ASSY

POWER SUPPLY BOARD ASSY SCH-7

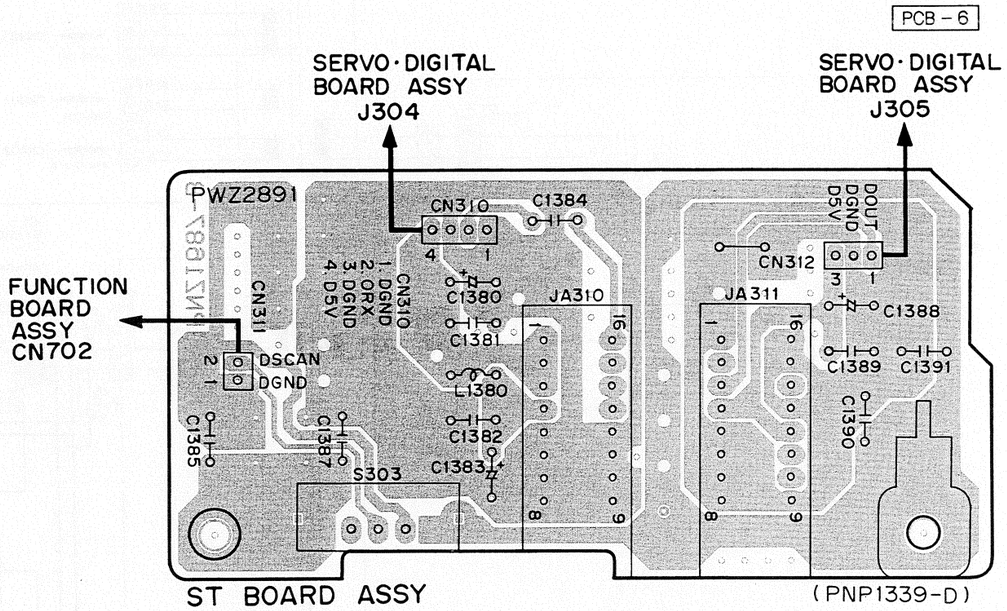
2.8 ST BOARD ASSY

ST BOARD ASSY (PWZ2891) SCH – 8



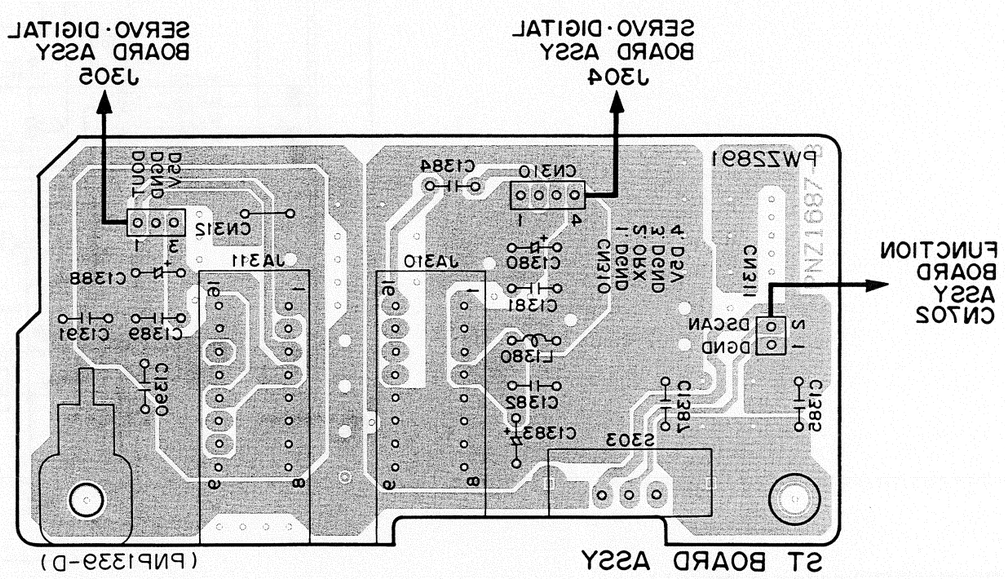
SCH-8 ST BOARD ASSY

PCB – 6



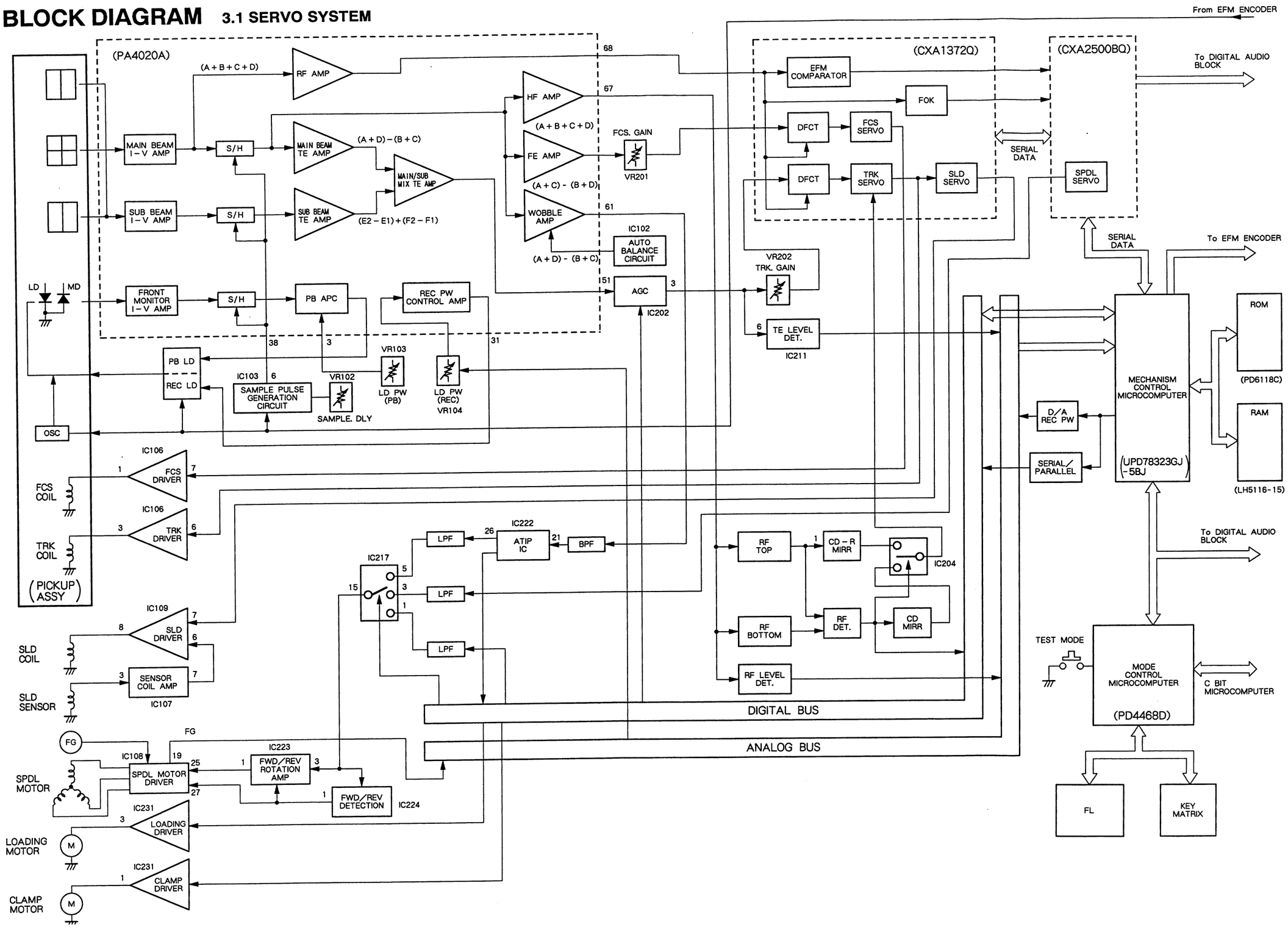
● This diagram is viewed from the mounted parts side.

PCB – 6

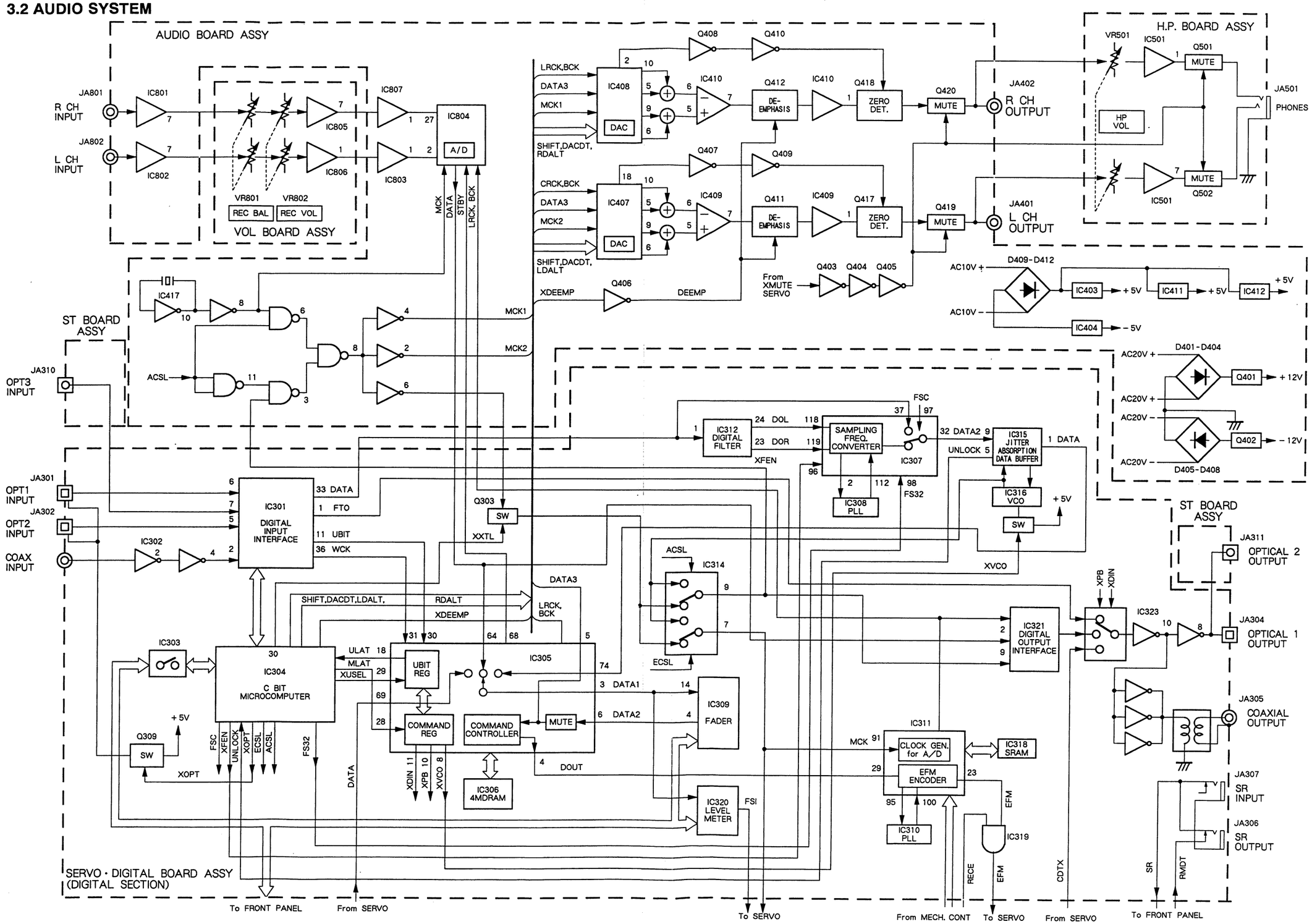


● This diagram is viewed from the foil side.

3. BLOCK DIAGRAM 3.1 SERVO SYSTEM



3.2 AUDIO SYSTEM



4318

PIONEER®
The Art of Entertainment

Service Manual

ORDER NO.
RRV1198

COMPACT DISC RECORDER
PDR-09

- **Refer to the service manual RRV1172 for PDR–09/KU.**

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	Remarks
	PDR–09		
WEM	○	AC220-240V	

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 300 Allstate Parkway Markham, Ontario L3R 0P2 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Haven 1087 Keetberglaan 1, 9120 Melsele, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

T-IFI NOV. 1994 Printed in Japan
4318

1. SAFETY INFORMATION

(FOR EUROPEAN MODEL ONLY)

VARO!
AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

ADVERSEL:
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

VARNING!
OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.

LASER
Kuva 1
Lasersateilyn
varoitusmerkki

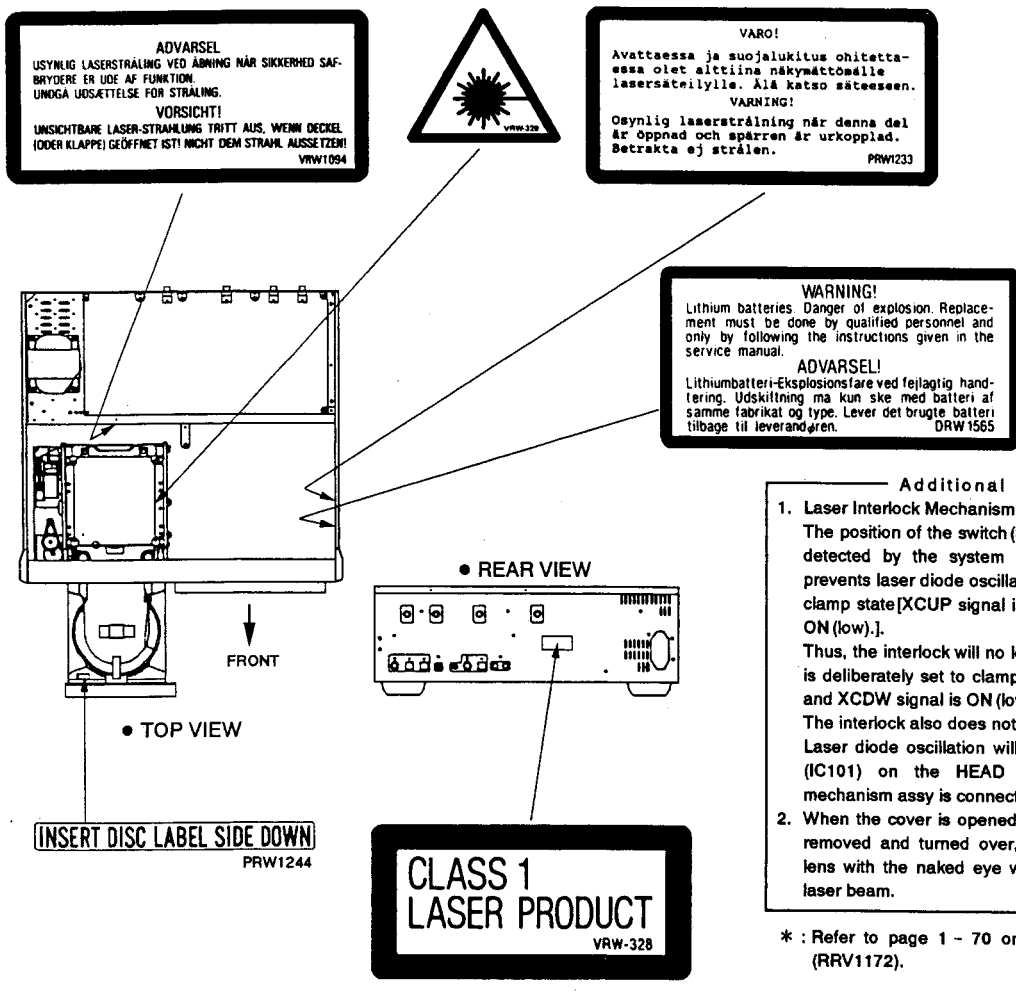
WARNING!
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS
MAXIMUM OUTPUT POWER: 30mw
WAVELENGTH: 780-785 nm

LASER
Picture 1
Warning sign for
laser radiation

LABEL CHECK



Additional Laser Caution

1. Laser Interlock Mechanism
   The position of the switch (S102) for detecting clamp state is detected by the system microprocessor, and the design prevents laser diode oscillation when the switch (S102) is not clamp state [XCUP signal is OFF (high) and XCDW signal is ON (low).].
   Thus, the interlock will no longer function if the switch (S102) is deliberately set to clamp state [XCUP signal is OFF (high) and XCDW signal is ON (low).].
   The interlock also does not function in the test mode ＊.
   Laser diode oscillation will continue, if pin 39 of PA4020A (IC101) on the HEAD assy mounted on the single mechanism assy is connected to GND.
2. When the cover is opened with the servo mechanism block removed and turned over, close viewing of the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

92TT1B

＊ : Refer to page 1 - 70 on the service manual PDR - 09 (RRV1172).

LITHIUM BATTERY NOTICE

WARNING!

Lithium batteries. Danger of explosion. Replacement must be done by qualified personnel and only by following the instructions given in the service manual.

This warning is stated on the product or in the operating instructions. When replacing the lithium batteries, follow the note below.
Dispose of the used battery promptly. Keep away from children. Do not disassemble and do not dispose of in fire.
The battery used in this device may present a fire or chemical hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Replace only with the same Part Number. Use of another battery may present a risk of fire or explosion.

Note: The lithium battery installation position is shown in the exploded view and the P.C. board pattern.

ADVARSEL!

Lithiumbatteri — Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

Denne advarsel or angivet på produktet eller i brugsvejledningen. Ved udskiftning af lithium batterierne følges nedenstående anveisning.
Batterierne må kun udskiftes med batterier af samme type og mærke.

VARNING!

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

Denna varning finns på apparaten eller i bruksanvisningen. Följ nedanstående anvisningar vid byte av litiumbatterier.
Batterierna får endast bytas ut mot litiumbatterier av samma typ och fabrikat.

2. CONTRAST OF MISCELLANEOUS PARTS

NOTES:
- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

• CONTRAST OF MISCELLANEOUS PARTS

PDR-09/KU and PDR-09/WEM have the same construction except for the following :

Mark	Symbol & Description	Part No.		Remarks
		PDR-09/KU	PDR-09/WEM	
	SERVO•DIGITAL BOARD ASSY	PWM1717	PWM1927	
	POWER BOARD ASSY	PWR1025	• • • • •	
NSP	POWER BOARD ASSY	• • • • •	PWR1027	
NSP	POWER SUPPLY BOARD ASSY	PWZ2461	• • • • •	
	POWER SUPPLY BOARD ASSY	• • • • •	PWZ2462	
NSP	ST BOARD ASSY	PWZ2891	• • • • •	
	FRONT BOARD ASSY	PWX1256	• • • • •	
NSP	FRONT BOARD ASSY	• • • • •	PWX1257	
NSP	FUNCTION BOARD ASSY	PWZ2464	• • • • •	
	FUNCTION BOARD ASSY	• • • • •	PWZ2463	

Mark	Symbol & Description	Part No.		Remarks
		PDR-09/KU	PDR-09/WEM	
⚠	AC power cord	PDG1015	• • • • •	
⚠	AC power cord with connector	• • • • •	PDH1003	No.6
	Cord stopper	CM-22C	• • • • •	
⚠	Inlet (2P)	• • • • •	PKP1007	No.1
⚠	Power transformer (servo)(AC120V)	PTT1292	• • • • •	
⚠	Power transformer (servo)(AC220V-240V)	• • • • •	PTT1290	
⚠	Power transformer (audio)(AC120V)	PTT1293	• • • • •	
⚠	Power transformer (audio)(AC220V-240V)	• • • • •	PTT1291	
⚠	Fuse (FU10 : 2A/125V)	VEK1019	• • • • •	
⚠	Fuse (FU10 : T1A/250V)	• • • • •	REK-100	
NSP	Warranty card	ARY1026	ARW-088	
	Caution label (lithium)	• • • • •	DRW1565	(＊1)
	65 label	ORW1069	• • • • •	
	FL sheet	PAM1663	PAM1621	
	Front panel KU	PAN1300	• • • • •	
	Front panel	• • • • •	PAN1294	
⚠	Connector assy (2P)	PDE1252	• • • • •	
	Connector assy (2P)	• • • • •	PDE1210	No.2
	Turn table sheet assy	PEA1174	PEA1183	
NSP	FL spacer	• • • • •	PEB1137	No.5
	CDR packing case KU	PHG2089	• • • • •	
	CDR packing case/WEM	• • • • •	PHG1990	
NSP	Main chassis K	PNA2175	• • • • •	
NSP	Main chassis B	• • • • •	PNA2050	
	AC cord plate	PNB1515	• • • • •	
NSP	F board shield	• • • • •	PNM1219	No.4
	Rear panel KU	PNS1046	• • • • •	
	Rear panel/WEM	• • • • •	PNS1045	
	CDR disc caution	PRM1031	PRM1039	
	Caution label HE	• • • • •	PRW1233	(＊1)
	ICP caution label	PRW1383	• • • • •	
	ICP caution label	PRW1384	• • • • •	
	Ferrite core	PTH1018	PTH1021	No.3
	Polyethylene bag	Z21-013	• • • • •	
NSP	Caution label (F)	• • • • •	VRW-328	(＊1)
	Caution label (G)	• • • • •	VRW-329	(＊1)
	Caution label	• • • • •	VRW1094	(＊1)
	Operating instructions (English)	PRB1221	• • • • •	
	Operating instructions (English, French, German, Italian)	• • • • •	PRE1192	No.7
	Operating instructions (Spanish, Swedish, Danish, Dutch)	• • • • •	PRF1068	No.8
NSP	Shield seal (16)	• • • • •	PNM1034	No.9
NSP	Shield seal (12.5)	• • • • •	PNM1120	No.10

Note 1 : The numbers in the remarks column correspond to the numbers on the exploded diagram. Refer to " • EXPLODED VIEWS".
(＊1) : For the putting of these labels, refer to the "LABEL CHECK" on page 2.

• SERVO·DIGITAL BOARD ASSY

PWM1717 and PWM1927 have the same construction except for the following :

Mark	Symbol & Description	Part No.		Remarks
		PWM1717	PWM1927	
	C1322, C1323	• • • • •	CCCCH101J50	
	R1337	• • • • •	RS1/10S000J	
	J304 Connector assy (4P)	PDE1254	• • • • •	
	J305 Connector assy (3P)	PDE1253	• • • • •	

• POWER SUPPLY BOARD ASSY

PWZ2461 and PWZ2462 have the same construction except for the following :

Mark	Symbol & Description	Part No.		Remarks
		PWZ2461	PWZ2462	
	CN6 Connector 2P	• • • • •	B2P3-VH	(*)
	J1 2mm pitch connector assy 11P	PDE1258	PDE1242	
⚠	Terminal	RKC-061	• • • • •	(*)

Note (*) : CN6 and terminal are mounted at the same position on the P.C. board.

• FUNCTION BOARD ASSY

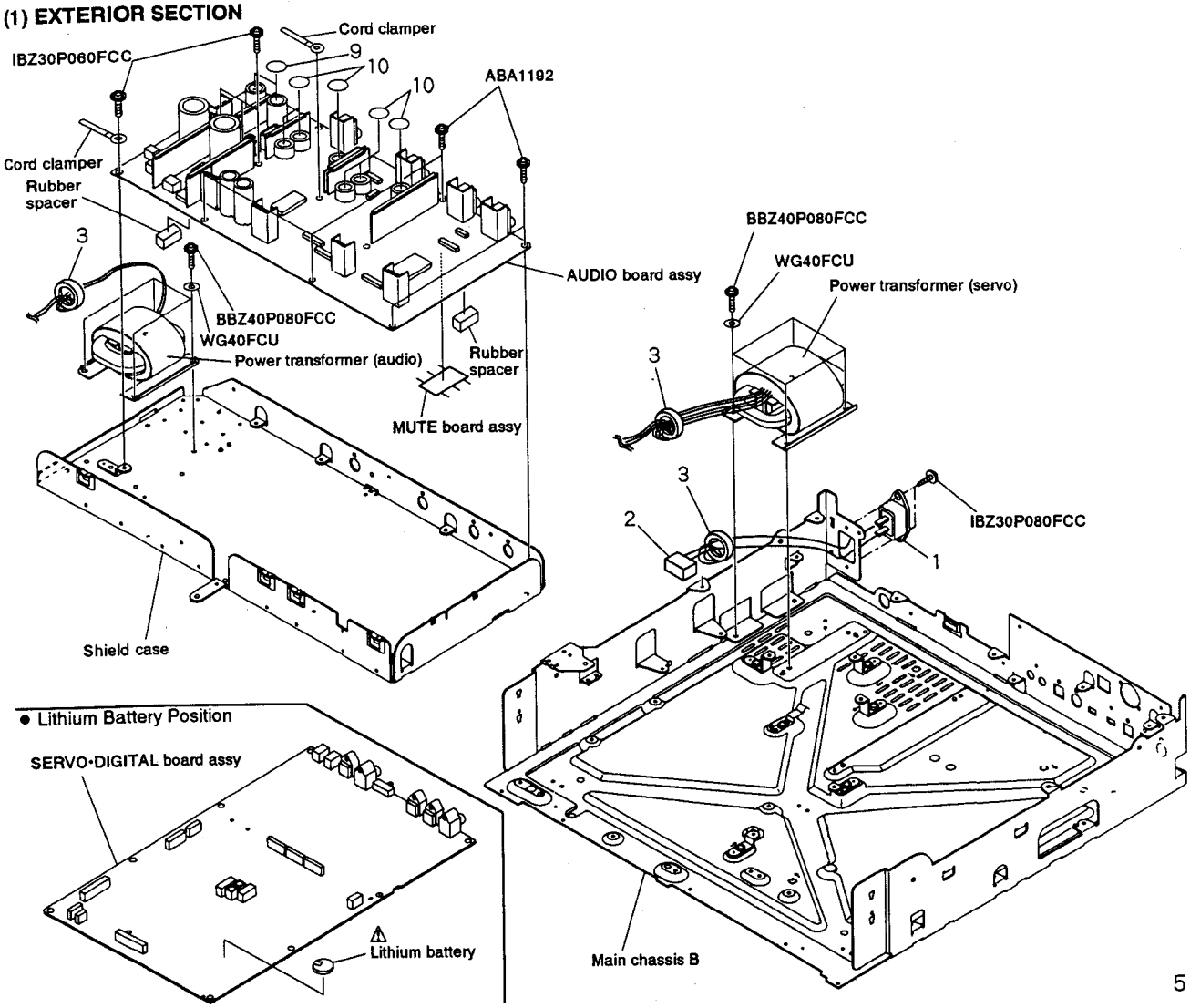
PWZ2464 and PWZ2463 have the same construction except for the following :

Mark	Symbol & Description	Part No.		Remarks
		PWZ2464	PWZ2463	
	CN702 Connector 2P	53025-0210	• • • • •	

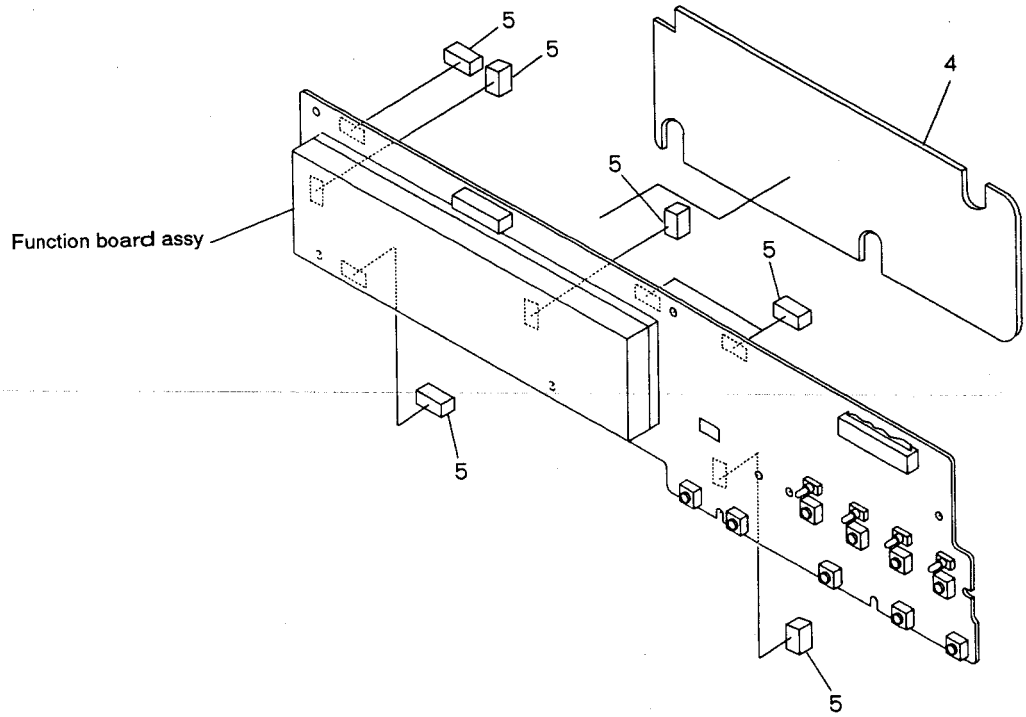
• EXPLODED VIEWS

Note : The numbers on the exploded diagram correspond to the numbers in the remarks column of the comparative table.
Refer to "CONTRAST OF MISCELLANEOUS PARTS".

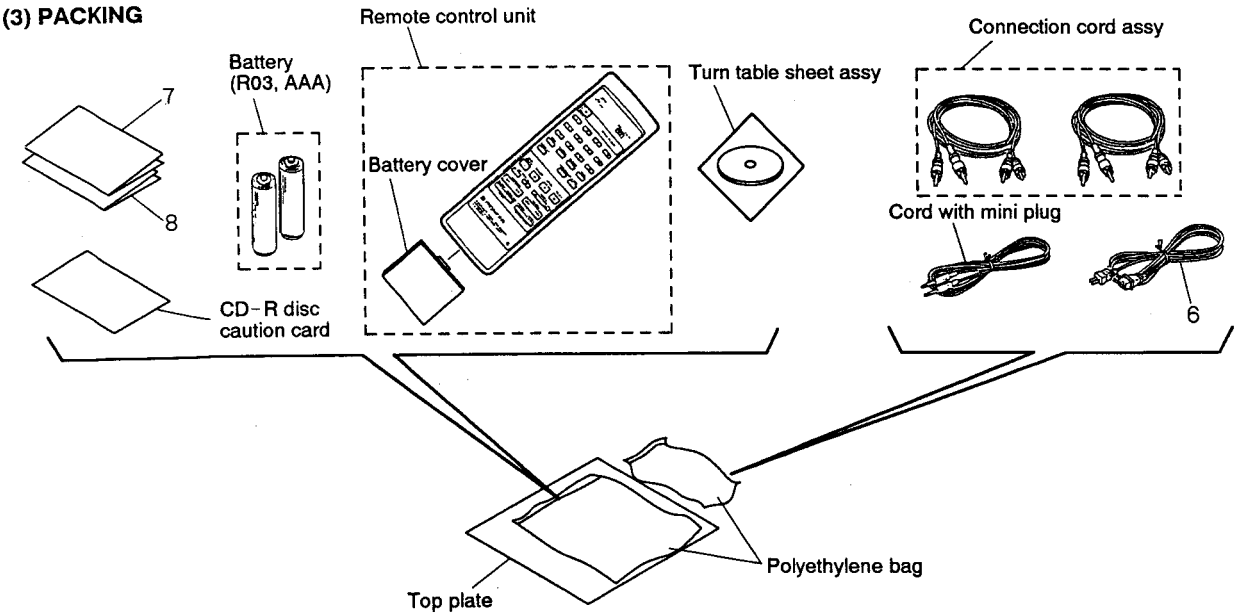
(1) EXTERIOR SECTION



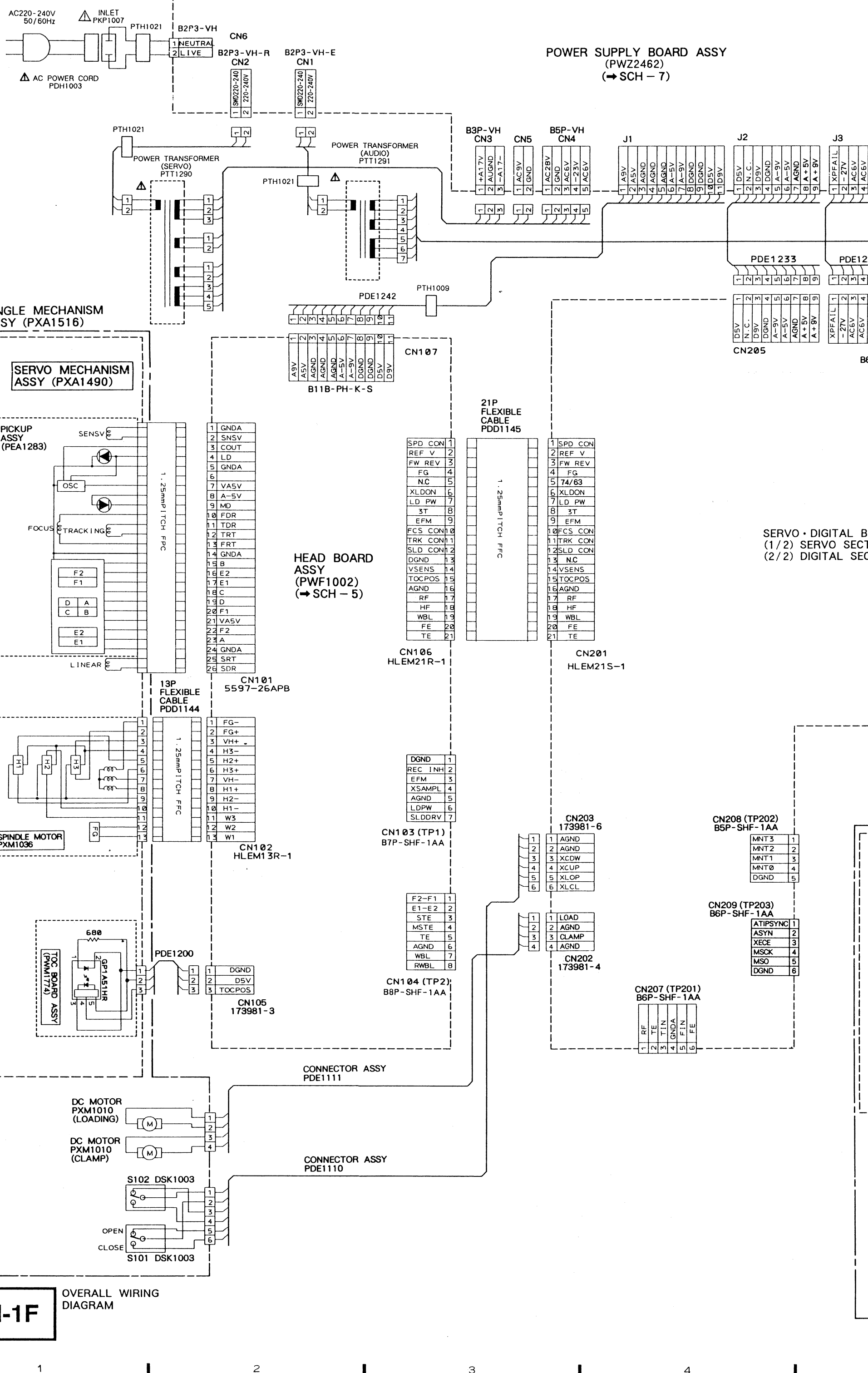
(2) FRONT SECTION



(3) PACKING



• SCHEMATIC DIAGRAMS
• OVERALL WIRING DIAGRAM



SCH-1F OVERALL WIRING DIAGRAM

SCH-1F

ER SUPPLY BOARD ASSY
(PWZ2462)
(➡SCH – 7)

J1 A9V A5V AGND AGND AGND A–5V A–9V DGND DGND DSV D9V
J2 D5V N.C. D9V DGND A–9V A–5V AGND A+5V A+9V
J3 XPFAIL –27V AC6V AC6V DA5V DGND

PDE1233 PDE1226

CN205 D5V N.C. D9V DGND A–9V A–5V AGND A+5V A+9V

CN204 B6B-PH-K XPFAIL –27V AC6V AC6V DA5V DGND

SR IN OUT
DIGITAL OUT OPTICAL COAXIAL
DIGITAL IN COAXIAL OPTICAL 1 OPTICAL 2

PDE1218
J301 DGND ADDATA DGND LRCK DGND ADBCK DGND ADLRCK DGND ADPD
CN802 DGND ADDATA DGND LRCK DGND ADBCK DGND ADLRCK DGND ADPD

CN401 +A20 +A20
CN403 B3P-VH +A10 CHASSIS –A10
–A20 –A20
LINE (ANALOG) OUT L R IN L R
CN402

PDE1231
CN406 B7B-PH-K MUTE HPROUT HPLOUT AUGND AU+12V AUGND AU–12V

PDE1219
J303 DGND DATA DGND BCK DGND ADMCK DGND MCK DGND ACSL
CN405 DGND DATA DGND BCK DGND ADMCK DGND MCK DGND ACSL

PDE1217
J302 DGND XDEEMP XMUTE XRESET LDALT RDALT SHIFT DACDT
CN404 B8B-PH-K DGND XDEEMP XMUTE XRESET LDALT RDALT SHIFT DACDT

AUDIO BOARD ASSY
(PWM1719)
(➡SCH – 4)

PDE1237
CN801 AUGND RVL IN RVLOUT AU–12V AUGND AU+12V LVLOUT LVL IN AUGND

SERVO · DIGITAL BOARD ASSY (PWM1927)
(1/2) SERVO SECTION (➡SCH – 2)
(2/2) DIGITAL SECTION (➡SCH – 2F)

CN201
LEM21S–1

CN206
HLEM22S–1
MREQ MACK XRESET FSCK FSO FSI CWORK UNLOCK CUREQ XRD CUACK CDR/CD LR XSOE ATTLAT RMDT SR DGND D5V AC6V AC6V –30V

1.25mmPITCH FFC
22P
FLEXIBLE CABLE
PDD1156

CN701
HLEM22R–1
MREQ MACK XRESET FSCK FSO FSI CWORK UNLOCK CUREQ XRD CUACK CDR/CD LR XSOE ATTLAT RMDT SR DGND D5V AC6V AC6V –30V

CN208 (TP202)
B5P-SHF-1AA
MNT3 MNT2 MNT1 MNT0 DGND

CN209 (TP203)
B6P-SHF-1AA
ATIPSYNC ASYN XECE MSCK MSO DGND

CN207 (TP201)
B6P-SHF-1AA
RF TE TIN GNDA FIN FE

DISPLAY SECTION

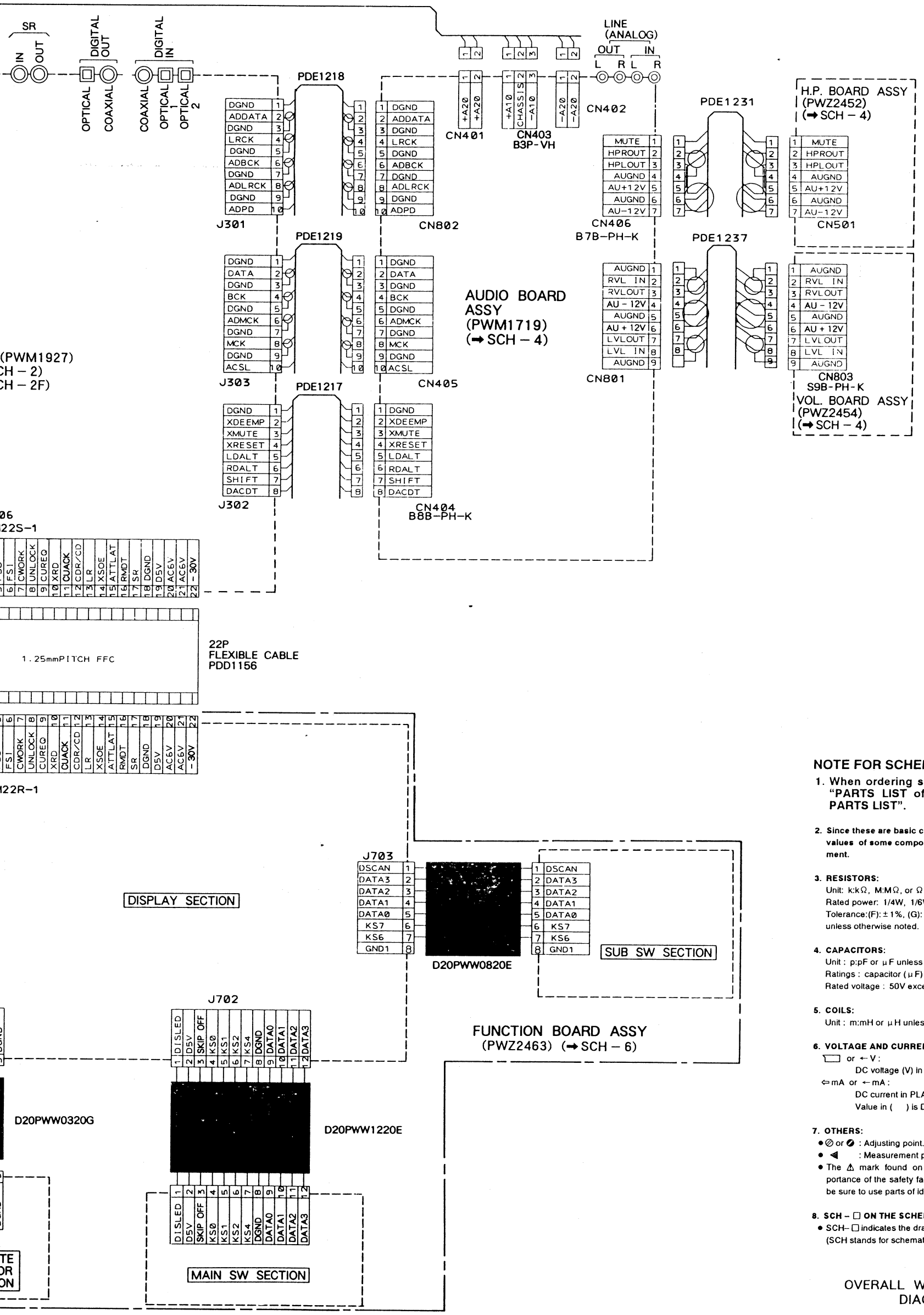
J703 DSCAN DATA3 DATA2 DATA1 DATA0 KS7 KS6 GND1
D20PWW0820E
SUB SW SECTION

FUNCTION BOARD ASSY
(PWZ2463) (➡SCH – 6)

J701 REMOTE D5V DGND
D20PWW0320G
REMOTE SENSOR SECTION

J702 DISLED D5V SKIP OFF KS0 KS1 KS2 KS4 DGND DATA0 DATA1 DATA2 DATA3
D20PWW1220E
MAIN SW SECTION

SCH-1F



NOTE FOR SCHEMATIC DIAGRAMS (Type 4A)

1. When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".
2. Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.
3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance:(F): ±1%, (G): ±2%, (K): ±10%, (M): ±20% or ±5% unless otherwise noted.
4. **CAPACITORS:**
   Unit : p:pF or μF unless otherwise noted.
   Ratings : capacitor (μF) / voltage (V) unless otherwise noted.
   Rated voltage : 50V except for electrolytic capacitors.
5. **COILS:**
   Unit : m:mH or μH unless otherwise noted.
6. **VOLTAGE AND CURRENT:**
   ▭ or ←V :
   DC voltage (V) in PLAY mode unless otherwise noted.
   ⇦mA or ←mA :
   DC current in PLAY mode unless otherwise noted.
   Value in ( ) is DC current in STOP mode.
7. **OTHERS:**
   - ⊘ or ⊘ : Adjusting point.
   - ◀ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.
8. **SCH - □ ON THE SCHEMATIC DIAGRAM:**
   - SCH-□ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram.)

OVERALL WIRING DIAGRAM **SCH-1F**

• SERVO · DIGITAL BOARD ASSY (2/2)

Q309 : POWER SW for OPTICAL INPUT TERMINAL

IC301 : INPUT SELECTOR & DIGITAL INTERFACE DECODER

IC302 (4/6) : INVERTER BUFFER

IC302 (6/6), (5/6) : LOOP FILTER

IC312 : DIGITAL FILTER

IC302 (1/6), (2/6): WAVE SHAPING

IC302 : TC74HCU04AP

IC303 SERIAL BUS SELECTOR

IC304 : C BIT μ-COM

IC305 MEMORY CONTROLLER

IC306 : 4M DRAM

IC308 : PLL

IC309 : DIGITAL FADER

IC310 : PLL

IC320 LEVEL METER INTERFACE

Q302 : INVERT BUFFER

Q303 : X'tal OFF

Q305-Q308 : MUTING CONTROL

Note ;
S : STOP state
P : PLAY state
R : REC state
STOP state unless otherwise noted.

SERVO SECTION (➡ SCH – 2)

AUDIO BOARD ASSY CN802 (➡ SCH – 4)

DIGITAL IN

IC312 : DIGITAL FILTER
IC312 SM5813AP
IC307 PD6093A FS CONVERETER
IC315 : JITTER CLEANER
IC315 M65811FP
IC317 (2/6) : LOOP FILTER
IC316 :
IC314 : MASTER CLOCK SELECTOR
IC314 TC74HC153AP
IC308 : PLL
IC308 MC74HC4046AN
Q303 : X'tal OFF
Q301 DTC144ES
IC317 (5/6) IC317 (4/6) IC317 (3/6) IC317 (6/6) : INVERTER BUFFER
IC313 (4/6) IC313 (5/6) IC313 (3/6) IC313 (2/6)
IC313 : TC74HC04AP
IC313 (3/6)–(5/6) : INVERTER BUFFER
IC313 (1/6),(6/6) : INVERTER BUFFER
IC318 GGF9002 (HM6264ALFP-12)
IC318 : 64k SRAM
IC320 PD2020 LEVEL METER INTERFACE
IC309 : DIGITAL FADER
IC309 PD0026A
IC310 MC74HC4046AN
IC310 : PLL
IC311 LC89583 EFM ENCODER
IC321 TC9231N
IC322 TC74HC153AP
IC322 : DIGITAL OUT SELECTOR
IC323 (1/6) TC74HC04AP
IC323 (1/6) - (6/6) : INVERTER BUFFER
IC319 TC7S08F
IC319 : EFM CONTROL
R1201-R1204 : 100
IC228 (MECH. CON) 64pin
P state
Y state
state
tate unless otherwise noted.

SERVO • DIGITAL BOARD ASSY (2/2) (PWM1927)

SCH-2F

• DIGITAL SECTION

➡ : PLAYBACK SIGNAL ROUTE
▨ : REC SIGNAL ROUTE

IC315 : JITTER CLEANER

IC315 M65811FP

IC317 (2/6) : LOOP FILTER

IC316 : VCO

IC316 PCX1021

Q304 DTA114ES

Q304 : VCO POWER SW

IC317 (1/6) TC74HCU04AP

IC317 (1/6) : INVERTER BUFFER

IC314 : MASTER CLOCK SELECTOR

IC314 TC74HC153AP

IC317 (3/6),(6/6) : INVERTER BUFFER

IC313 (3/6)

IC313 (2/6)

IC313 : TC74HC04AP

IC313 (1/6),(6/6) : INVERTER BUFFER

IC313 (6/6)

IC313 (1/6)

IC318 : 64k SRAM

IC322 : DIGITAL OUT SELECTOR

IC322 TC74HC153AP

IC323 (6/6)

IC323 (5/6)

IC323 (4/6) DTF1067

IC323 (1/6) TC74HC04AP

IC323 (2/6)

IC323 (3/6)

IC323 (1/6) - (6/6) : INVERTER BUFFER

IC321 TC9231N

IC321 : DIGITAL INTERFACE ENCODER

IC311 LC89583 EFM ENCODER

IC319 TC7S08F

IC319 : EFM CONTROL

J303 PDE1219

J302 PDE1217

AUDIO BOARD ASSY CN405 (➡ SCH – 4)

AUDIO BOARD ASSY CN404 (➡ SCH – 4)

DIGITAL OUT OPTICAL

JA304 TOTX178

S301 RSH1025

DIGITAL OUT OFF

DIGITAL OUT COAXIAL

JA305 RKB1012

SR IN JA307 PKN1004

SR JACK

SR OUT JA306 PKN1004

IC228 (MECH. CON) 64pin

R1201-R1204 : 100

IC313 : TC74HC04AP

SERVO • DIGITAL BOARD ASSY (2/2)

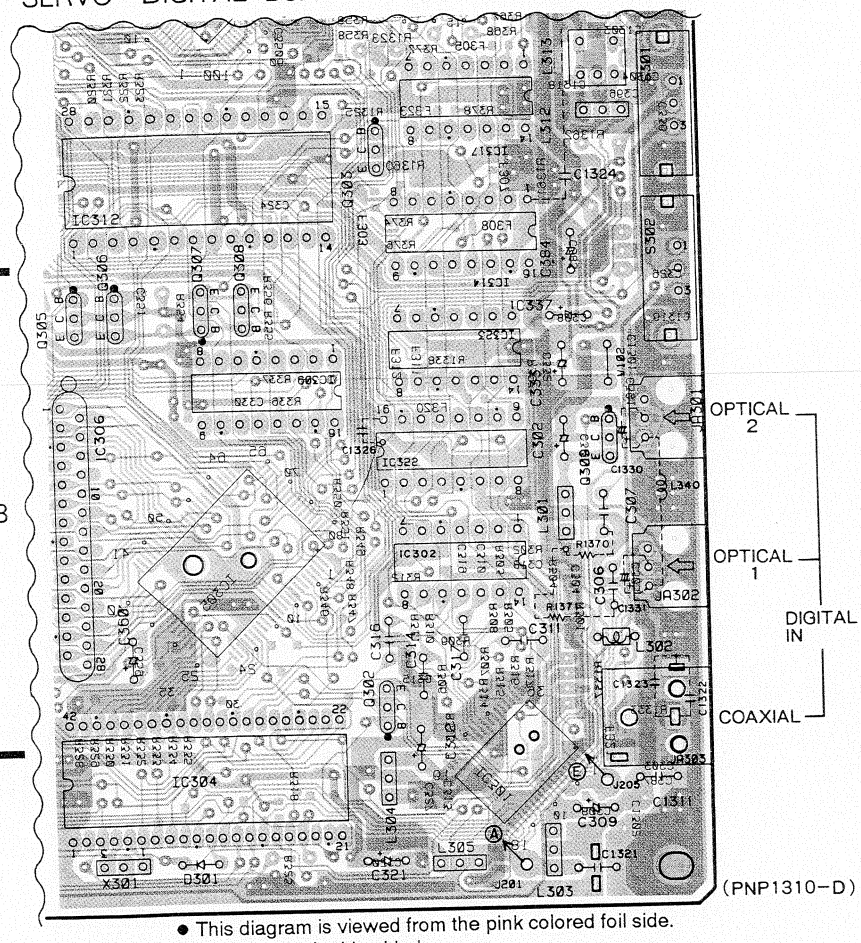
SCH-2F

• PCB DIAGRAM

• The differences in the PCB diagram between PWM1717 and PWM1927 are as follows.

PCB – 1F

SERVO • DIGITAL BOARD ASSY



• This diagram is viewed from the pink colored foil side.
• This PCB is double sided.

NOTE FOR PCB DIAGRAMS:
1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator

• LITHIUM BATTERY POSITION